

LPA11

LPA/KW11-K TEST
CRLPGCO

AH-B038C-MC
FICHE 1 OF 1

FEB 1981
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The main body of the document is a large grid of approximately 15 columns and 25 rows of data. Each cell in the grid contains a small, dense table or set of data points. The text is very small and difficult to read, but the overall structure is a comprehensive data matrix. The data appears to be organized in a regular, repeating pattern across the grid.

Identification

SEQ 0001

Product Code: AC-B037C-MC
Diagnostic Code: MAINDEC-11-CRLPG-C
Product Name: CRLPGCO LPA/KW11K TEST
Date Revised: DEC. 1980
Maintainer: DIAGNOSTIC ENGINEERING

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1.0 ABSTRACT *****

"C" VERSION OF THE PROGRAM IS DUE TO A CHANGE IN THE MICRO-CODE IN THE LPA-11 (DMC-11).
"B" VERSION OF THE PROGRAM FIXES LS210 THRU LS230 PROGRAM BUGS AND SEVERAL DOCUMENTATION ERRORS.

This program allows the user to check out or debug the KW11K, DUAL REAL TIME CLOCK. The logic test is self contained and needs no external maintenance hardware or operator intervention.

Five special tests are included within this program to allow the user to check out and debug the external I/O signals. To run these tests a jumper wires is needed in order to loop output to an input.

THIS PROGRAM IS A MODIFIED VERSION OF 'MD-11-DZKWK-A'. IT WAS MODIFIED TO ENABLE THE OPERATOR TO CHECK OUT THE KW11K OPTION WHEN IT IS ON THE LPA11-KX I/O BUS. NO RECALING IS NEEDED. SOME TEST DONE IN THE ORIGINAL DIAGNOSTIC SUCH AS ARBRITRATION TEST, WERE DELETED AS THEY COULD NOT BE CHECKED. IF THIS DIAGNOSTIC DOESN'T FIND A SUSPECTED PROBLEM, YOU MAY HAVE TO RUN 'MD-11-DZKWK-A'. YOU SHOULD RUN 'MD-11-CRLPA' BEFORE RUNNING THIS DIAGNOSTIC. PLEASE READ SECTION 10.

2.0 REQUIREMENTS *****

2.1 Equipment

1. PDP11 FAMILY COMPUTER with 16K of memory or more and I/O facilities (a switch register or TTY).
2. KW11K under test installed in the LPA-11KX.
3. For external I/O signal tests a loopback wire (Jumper) is needed. Jumpers are 30 AWC jumper type 915.
4. LPA11-KX

2.2 Storage

This program occupies and uses only the lower 16K of memory.

3.0 LOADING PROCEDURE

*****~*****

3.1 Method

Standards procedure for normal binary tapes should be followed.

1. Absolute loader must be in memory.
2. Place binary tape in reader.
3. Load address *7500 (* determined by location of loader).
4. Press "Start" (program will be loaded into memory).

The program can also be loaded by XXDP, ACT, or APT.

3.2 Non-Standard Address, Vector, or Priority; or Use of Software Switch Register

This program is set to test a KW11K with a standard address, vector, and priority. If any of these are different on the KW11K you are testing, change the corresponding location in memory before starting this test.

<u>LOCATION</u>	<u>TAG</u>	<u>CURRENT CONTENTS</u>	<u>COMMENTS</u>
1254	\$BASE:	170404	::Base address of equipment :: under test
1250	\$VECT1:	000344	::INTERRUPT Vector #1
1252	\$PRIOR:	000006	::Bus priority - 1,#2
176	\$SWREG:	000000	::Manual SWR.
	\$TPFLG:	.BYTE 0	::"Terminal Available" : Flag (Bit<0:7>=0=Yes)

NOTE

If no hardware Switch Register exists, you may set any bit in "SWREG" as you would have set it in the SWR.

4.0 STARTING PROCEDURE *****

4.1 Control Switch Settings

Starting at memory locations 200, 204, 210, 214, 220, 224, 230 or 234, set all switches as desired. See Section 5.1.

4.2 Starting Addresses

200	Start address for logic test.
204	Restart address for logic test.
210	Start address for "STP2 OUT", "SCHMITT TRIG 1" tests.
214	Start address for "STP1 OUT", "SCHMITT TRIG 2" tests.
220	Start address for "SCHMITT TRIG 3 IN", "ST3 OUT" tests.
224	Starting address for "A EVENT OUT" test.
230	Starting address for "B EVENT OUT" test.
234	Starting address for "USER LINK" loop.

4.3 Program AND/OR Operator Action

1. Load program into core.
2. Set switch register to starting address.
3. Load address.
4. Set switches to desired settings - see section 5.1.
5. IF starting a special I/O signal test:
MAKE WIRE LOOP CONNECTION.
6. Press Start.

5.0 OPERATING PROCEDURE *****

5.1 Switch Register Function

Switch use -----

15 Halt on error
14 Loop on test
13 Inhibit error typeout (all tests)
13 Inhibit "*" typeout (special I/O signal tests)
10 Bell on error
9 Loop on error
8 Loop on test in SWR <7:0>

5.2 Scope Loops

If an error occurs and the user wishes to scope the error, he (or she) should set SW15=1 to halt on error, then when the program halts on error, SW15=0, set SW14=1. To loop on current test, set SW13=1 to inhibit error printout, and press continue on the CPU's console.

NOTE

For each test in the listing, you will find a test description. In each description a probable SYNC Point is listed. These Points are listed AS A GUIDE in order for you to SYNC your scope to the Signals being generated.

5.3 Program AND/OR Operator Action

5.3.1 Logic Test

For each pass through the program 'END PASS' will be printed out at the end of a pass.

If not inhibited by APT, the program will look for more KW11Ks to exercise, one pass will exercise all KW11Ks.

5.3.2 Special I/O Signal Tests

There are no "Short Passes". Each pass will iterate 65,324 times. A "*" is typed at the end of a pass unless SW13=1.

6.0 ERRORS *****

SEQ 0007

6.1 Error Printout

Printout varies with the error detected. The error PC typed out is the actual location of the error call.

A halt at location '\$TYPE'+10 when running with no terminal indicates an error has occurred. To find out the number of the error, examine location '\$STNM'. This is the item number of the error. To find out what the error typout would have been GOTO to the error pointer table beginning at location '\$ERRTB'.

6.1.1 Example

If we examined location '\$STNM' and found a 5 (101) we go to location '\$ERRTB' and look through the error pointer table until we found item 5. The information would look like:

```
;ITEM 5
      EMS           ;CLOCK B SR DATA ERROR
      DHS           ;ERRPC  BSR      WAS      S/B
      DT5           ;$ERRPC,BSR,$BDDAT,$GDDAT
      DFO           ;ALL NUMBERS ARE IN OCTAL FORM
```

To find out the information specified by DT5 (\$ERRPC,BSR,\$GDADR,\$BDADR) follow these steps:

1. Look up the address of the label (i.e., \$ERRPC) in the symbol table which follows the listing.
2. Put this address in the witch register and depress the load address switch on the processor's console.
3. Now depress the Examine switch.
4. The data displayed in the data lights is the information that would have been printed for this label if you had a input/output terminal.

6.2 Non-Standard Error HALTS

A HALT MAY OCCUR IF THE PROGRAM DETECTS AN LPA11-KX ERROR.
CHECK THE COMMENTS IN THE LISTING OPPOSITE THE PC HALT.

7.0 RESTRICTIONS *****

Jumper W2 must be installed if not jumpered on module.
JUMPER W3, W4, AND W5 MUST BE INSTALLED TO RUN SIGNAL TESTS.

Logic Test must be run before any special I/O Signal Test.

The program is chainable under XXDP. However only one pass may be made (R RLPGC0/1).

8.0 MISCELLANEOUS *****

After a power failure occurs, program execution will NOT continue at the point where the power failure occurred.
The program will be restarted.

This program is chainable under XXDP, ACT, or APT.

Logic Test

90 SECONDS if no errors.

8.3.2 Special I/O Signal Tests

1.0 Minutes No errors, SW13=0.

Execution times are approximate, as the various PDP-11 CPU's have varied instruction execution times.
Times quoted were taken from a run on a PDP-11/34.

8.4 USER LINK TO I/O DEVICE

A SPECIAL USER LINK HAS BEEN PROVIDED IN ORDER FOR THE OPERATOR TO EXAMINE OR MODIFY LOCATIONS ON THE LPA11-KX I/O BUS. (NOTE: THIS CANNOT BE DONE DIRECTLY.)

PROCEDURE:

- 1) START THE PROCESSOR AT LOCATION 234
- 2) THE DIALOG TO EXAMINE A LOCATION IS AS FOLLOWS:

```
E OR D      'E'  
DEVICE ADDR= 'OCTAL ADDRS'  
XXXXXX
```

WHERE XXXXXX IS THE CONTENTS OF THE SPECIFIED LOC.

- 3) THE DIALOG TO MODIFY A LOCATION IS AS FOLLOWS:

```
E OR D      'D'  
DATA=       'DATA TO BE DEPOSITED'
```

- 4) THE PROGRAM WILL STAY IN THIS LOOP UNTIL THE OPERATOR IS FINISHED. AT THIS TIME THE PROCESSOR SHOULD BE HALTED.

NOTE: THE OPERATORS RESPONSE IS ENCLOSED IN QUOTES.

9.0 PROGRAM DESCRIPTION *****

9.1 Logic Tests

A complete description of each test is included withing the listing before each test.

9.2 Special External I/O Signal Tests

9.2.1 LS210 "STP2 OUT" to "SCHMITT RIG 1 IN" Tests

This is a special section devoted for testing and providing scope loop capabilities for "STP2 OUT" L and "SCHMITT TRIG 1" IN.

When you load and start at location 210, program control is transferred here. "STP2 OUT" L pulses are generated by 'LD STAT A HI' H + 'BD10' H (Main. STP2).

Pin V ("STP2 OUT") is wired to pin LL (SCHMITT TRIG1) for this test. "STP2 OUT" pulses are received as "SCHMITT TRIG 1" pulses which set clock A's status register bit 15. If an error is detected, normal error reporting technique, and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins V and LL of J1 together.
Jumper W3 must be INSTALLED.

Logic test (L + S 200) should be run first.

9.2.2 LS214 "STP1 OUT" to "SCHMITT RIG 2" H Tests

This is a special test section devoted for testing and providing scope loop capabilities for "STP2 OUT" and "SCHMITT TRIG2" IN.

When you load and start at location 214, program control is transferred here. "STP1 OUT" L pulses are generated by 'LD STAT A HI' + 'BD12' H (min S). Pin DD ("STP1 OUT") is wired to pin BB ("SCHMITT TRIG 2") for this test. "STP1 OUT" pulses are received as "SCHMITT RIG 2" pulses which will clear clock A's count register if mode 3 is selected. If an error is detected, normal error reporting technique, and error switch register options are used. An "*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD and BB of J1 together.
Jumper W4 must be installed.

Logic tests (L + S at 200) should be run first.

9.2.3 LS220 'SCHMITT TRIG 3' in, 'ST3 OUT' Tests

This is a special section devoted for testing and providing scope LOOPS CAPABILITIES FOR 'SCHMITT TRIG 3' AND 'ST3 OUT'.

When you load and start at location 220, program control is transferred here. 'STP1' pulses are generated by 'LD STAT A H,' + 'BD12' H (main STP1). Pin dd ('STP1 OUT') is wired to pin T ('SCHMITT RIG 3'). 'SCHMITT TRIG 3' pulses give us 'ST3 OUT' pulses. Pin L ('ST3 OUT') is wired to pin BB ('SCHMITT TRIG2'), and 'SCHMITT TRIG 2' will set clock A's status register bit 7.

If an error is detected, normal error reporting technique, and error switch register options are used. An '*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD to T of J1 together, as well as pins L to BB of J1 together. Jumpers W4 and W5 must also be installed.

Tests LS210 and LS214 should be run first.

9.2.4 LS224 'A EVENT OUT' Test

This is a special section devoted for testing and providing scope loop capabilities for 'A EVENT OUT'.

When you load and start at location 224, program control is transferred here. 'A EVENT OUT' pulses are generated by clock A overflows. Pin VV ('A EVENT OUT') is wired to pin BB ('SCHMITT TRIG 2'). 'SCHMITT TRIG 2' pulses will set clock A's CSR bit 7. If an error is detected, normal error reporting technique, and error switch register options are used. An '*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins VV and BB of J1 together. Jumper W4 must also be installed.

Test LS210 should be run first.

9.2.5 LS230 'B EVENT OUT' Test

This is a special section devoted for testing and providing scope loop capabilities for 'B EVENT OUT'.

When you load and start at location 230, program control is transferred here. 'B EVENT OUT' pulses are generated by clock B overflows. Pin TT ('B EVENT OUT') is wired to pin BB ('SCHMITT TRIG 2'). 'SCHMITT TRIG 2' pulses will set clock A's CSR bit 7. And error switch register options are used. An '*' is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins TT and BB of J1 together. Jumper W4 must be installed also.

Test LS210 should be run first.

10.0 LPA11 (SYSTEM) DIAGNOSTIC SUMMARY

DIAGNOSTICS FOR THE LPA11 ARE WRITTEN AT THREE LEVELS: (1) TOTAL PDP-11 SYSTEM, (2) LPA11 SYSTEM; AND, (3) LPA11 OPTIONS.

LEVEL 1, IS DESIGNED TO ISOLATE A FAILURE TO THE LPA11 SYSTEM. ALL OPTIONS ON THE PDP-11 ARE EXERCISED.

LEVEL 2 DIAGNOSTICS ISOLATE A FAILURE TO THE INDIVIDUAL OPTION WITHIN THE LPA11. THE LEVEL 2 DIAGNOSTIC IS MD-11-DRLPA. WHEN THE USER RUNS DRLPA HE CAN GENERALLY TELL WHICH OPTION DIAGNOSTIC (LEVEL 3) TO RUN NEXT. M8254 AND M8200-YC ERRORS MAY "LOOK" ALIKE AND DRLPA MAY NOT BE ABLE TO DISTINGUISH BETWEEN THEM. ARBITRATION ERRORS WILL NOT BE DETECTED BY THIS DIAGNOSTIC.

LEVEL THREE DIAGNOSTICS AID IN DETERMINING IF THE ERROR WAS IN FACT ON THE OPTION THE DRLPA SPECIFIED. THE USER MAY "LOOP" ON THE ERROR. WITHIN LEVEL THREE, THERE ARE TWO GROUPS OF DIAGNOSTICS. THE FIRST GROUP REQUIRES NO "EXTRA" WORK BY THE USER IN ORDER TO RUN. GROUP "A" DIAGNOSTICS DO NOT CHECK ARBITRATION, AND REQUIRE EXTRA TIME FOR EXECUTION. THE SECOND GROUP (GROUP "B") REQUIRES THAT THE USER RECONFIGURE THE PDP-11 SYSTEM. THIS RECONFIGURATION INVOLVES CABLING THE UNIBUS TO THE LPA'S I/O BUS.

THE DIAGNOSTIC FOR THE M8254 FALLS INTO THE GROUP "B" CATEGORY.

THE LPA11-KX DIAGNOSTIC KIT WILL INCLUDE:

<u>OPTION</u>	<u>GROUP</u>	<u>DIAG. #</u>	<u>DIAG. TITLE</u>
LPA11-KX	LEVEL 2	MD-11-CRLPA	LPA11-K SYSTEM EXER.
M8254	'B'	MD-11-CRLPM	M8254 (IPBM) FIELD DIAG.
AA11-K	A	MD-11-CRLPB	LPA/AA11-K DIAG.
	B	MD-11-DZAAC	AA11-K DIAG.
AR11	A	MD-11-CRLPC	LPA/AR11 DIAG. #1
	A	MD-11-CRLPD	LPA/AR11 DIAG. #2
	A	MD-11-CRLPE	LPA/AR11 DIAG. #3
	B	MD-11-DZARA	AR11 DIAG. #1
	B	MD-11-DZARB	AR11 DIAG. #2
	B	MD-11-DZARC	AR11 DIAG. #3
DR11-K	A	MD-11-CRLPF	LPA/DR11-K DIAG.
	B	MD-11-DZDRG	DR11-K DIAG.
KW11-K	A	MD-11-CRLPG	LPA/KW11-K DIAG.
	B	MD-11-DZKWK	KW11-K DIAG.
LPS-11	A	MD-11-CRLPH	LPA/LPS11 DIAG. #1
	A	MD-11-CRLPI	LPA/LPS11 DIAG. #2
	A	MD-11-CRLPJ	LPA/LPS11 DIAG. #3
	B	MD-11-DZLPC	LPS11 DIAG. #1
	B	MD-11-DZLPD	LPS11 DIAG. #2
	B	MD-11-DZLPI	LPS11 DIAG. #3
AD11-K	A	MD-11-CRLPK	LPA/AD11-K DIAG.
	B	MD-11-DZADL	AD11-K DIAG.
M8200-YC	B	MD-11-CRLPL	LPA/DMC-11 DIAG. TST I
	B	MD-11-CRLPM	LPA/DMC-11 DIAG. TST II

THIS IS A HISTORY FILE OF CRLPG-C

 THE 'C' VERSION SOURCE ONLY HAS THE B TO C VERSION CHANGES
 THE BIG CHANGE IS IN THE 'CRLPA.MAC' FILE THAT HANDLES THE
 NEW VERSION OF THE MICRO-CODE IN THE LPA-11

THE 'A' VERSION HAD SEVERAL PROBLEMS WHEN DEALING WITH LS204
 AND LS210 THRU LS230. THE FIRST WAS THAT LS204 FAILED TO CLEAR
 A LOCATION ".DVLS", WHICH INDICATED THE MICRO-CODE WAS LOADED
 AND RUNNING <AFTER A RESTART IS IS NOT RUNNING DUE TO "INIT">.
 THIS PROBLEM IS ALSO COMMON TO LS210 THRU LS230.
 THE SECOND PROBLEM IS THAT LS210 HAD A DESIGN FLAW <REALLY ONLY A
 ONE LINE TYPING REVERSAL> JAN 1979 R. SHOOP

HISTORY FILE OF DRLPG-A

 PRODUCT CODE: MAINDEC-11-DZKWK-A
 PRODUCT NAME: KW11-K DIAGNOSTIC TEST
 DATE: FEBRUARY 1976
 MAINTAINER: DIANOSTIC GROUP

PRODUCT CODE: MAINDEC-11-DRLPG-A
 PRODUCT NAME: LPA/KW11-K DIAGNOSTIC TEST
 DATE: JANUARY 1978
 MAINTAINER: DIAGNOSTIC GROUP

REASON FOR DEVELOPMENT:

1) TO ENABLE THE OPERATOR TO CHECK OUT THE KW11-K OPTION
 WHEN IT IS ON THE LPA11-KX I/O BUS.

CHANGES MADE:

- 1) TOOK OUT CERTAIN TESTS FROM ORIGINAL DIAGNOSTIC (I.E.
 INTERRUPTS, TIME DEPENDENT CODE).
- 2) REPLACED DIRECT LINKS TO DEVICE WITH MACRO CALLS TO THE
 KMC-11 MICRO CODE. KMC-11 MICRO CODE (FILE:DRLPX2) HANDLES
 DIRECT COMMUNICATIONS WITH THE DEVICE.

FILE: DRLPA.MAC
 CONTAINS MACRO LINKS BETWEEN PDP-11 CODE AND KMC-11
 MICRO CODE. FILE: DRLPX2 NEEDS TO BE ASSEMBLED WITH
 DRLPG (SEE .CTL FILE).

FILE: DRLPX2
 MICRO CODE FILE THAT GETS LOADED INTO THE KMC-11
 VIA ROUTINES IN DRLPA.MAC.
 DRLPX2.P11 IS ASSEMBLED WITH MACY11 (ONLY) AS ANY OTHER
 .P11 FILE. THE RESULTS OF ITS ASSEMBLY IS A .OBJ
 MODULE AS WAS THE RESULT OF THE ASSEMBLY OF THE
 DIAGNOSTIC .P11 FILE. BOTH .OBJ FILES GET LINKED
 WITH LNKX11 (ONLY).

FILE: DRLPG.CTL
 THIS FILE EXPLAINS SEQUENCE OF ASSEMBLES AND LINKS.
 IT IS IN TOPS-20 FORMAT.

LNKX11 V023 24-OCT-80 9:45

C 2

SEQ 0015

#CRLPGC.BIN/B:42000,CRLPGC.MAP=CRLPGC,CRLPX2/E

LOAD MAP

IDENT: V1015B

TRANSFER ADDRESS: 000001

LOW LIMIT: 042000

HIGH LIMIT: 046000

MODULE	LPA	ADDRESS	SIZE
SECTION	ENTRY		
<. ABS.>		000000	000000
	DRLPX2	042000	
<	>	042000	000000

MODULE	DRLPX2	ADDRESS	SIZE
SECTION	ENTRY		
<	>	042000	000000
<ABCODE>		042000	004000

RUN-TIME: 1 SECONDS

2K CORE USED

1208	OPERATIONAL SWITCH SETTINGS
1209	TRAP CATCHER
1220	BASIC DEFINITIONS
1275	ACT11 HOOKS
1277	APT PARAMETER BLOCK
1279	COMMON TAGS
(2)	APT MAILBOX-ETABLE
(1)	ERROR POINTER TABLE
1440	PROGRAM START
1444	INITIALIZE THE COMMON TAGS
1489	*
1490	* PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
1491	*
1518	T1 *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
1542	T2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
1571	T3 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
1604	T4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
1630	T5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WROTE/READ
1655	T6 *TEST THAT CLOCK B'S BUFFER REGISTER CAN BE WROTE/READ
1778	T7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
(5)	T10 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(5)	T11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(5)	T12 *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
(5)	T13 *TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED
(5)	T14 *TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(5)	T15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(5)	T16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(5)	T17 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(5)	T20 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(5)	T21 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(5)	T22 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T26 *TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T27 *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T31 *TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(6)	T33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
(6)	T34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
(6)	T35 *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(6)	T36 *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
(6)	T37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(6)	T40 *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(6)	T41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
(6)	T42 *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(6)	T43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(6)	T44 *TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
(6)	T45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T47 *TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T51 *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T52 *TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T53 *TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED

(6)	T54	*TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(6)	T55	*TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(6)	T56	*TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(6)	T57	*TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(6)	T60	*TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(6)	T61	*TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(6)	T62	*TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(6)	T63	*TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
1779	*	
1780	*	PHASE 2 ADVANCED BASIC LOGIC TESTS
1781	*	
1789	T64	*TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
1812	T65	*TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
1840	T66	*TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
1874	T67	*TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
1898	T70	*TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN
1926	T71	*TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
1968	T72	*TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
1998	T73	*TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. STP1
2034	T74	*TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
2083	T75	*TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1'S
2130	*	
2131	*	PHASE 3 CLOCK A COUNT FUNCTION TESTS
2132	*	
2144	T76	*TEST THAT CLOCK A OVERFLOW WILL OCCUR
2190	T77	*TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF 'ENB CNTR' F/F
2281	T100	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1
2282	T101	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
2283	T102	*TEST THE ABILITY OF CLOCK A TO COUNT AT 10KHZ RATE PART 1
2284	T103	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
2285	T104	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
2286	T105	*TEST THE ABILITY OF CLOCK A TO COUNT AT LINE-FREQ RATE PART 1
2297	T106	*TEST THAT CLOCK A DOESN'T COUNT WHEN NO RATE IS SELECTED
2339	T107	*TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
2379	T110	*TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
2418	T111	*TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE 2 OVERFLOW
2467	T112	*TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
2548	T113	*TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
2549	T114	*TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
2593	T115	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENERATED
2594	T116	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENERATED
2607	T117	*TEST THAT MODE 3 + 'STP2' CLEARS A'S COUNT REGISTER.
2651	T120	*TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
2724	T121	*TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
2756	*	
2757	*	PHASE 4 CLOCK B COUNT FUNCTION TESTS
2758	*	
2776	T122	*TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
2827	T123	*TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW
2893	T124	*TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
2943	T125	*TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.
2968	T126	*TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED
3048	T127	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
3049	T130	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
3050	T131	*TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
3051	T132	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1

3052	T133	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
3053	T134	*TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1
3064	T135	*TEST THE 'FEED B TO A' 24 BIT COUNTER FEATURE OF CLOCKS A + B
3113	*	
3114	*	PHASE 6 CLOCK A+B ADVANCE TESTING
3115	*	
3136	T136	*TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER
3258	T137	*TEST CLOCK A'S 100KHZ DIVIDER
3259	T140	*TEST CLOCK A'S 10KHZ DIVIDER
3260	T141	*TEST CLOCK A'S 1KHZ DIVIDER
3261	T142	*TEST CLOCK A'S 100HZ DIVIDER
3362	T143	*TEST CLOCK B'S 100KHZ DIVIDER
3363	T144	*TEST CLOCK B'S 10KHZ DIVIDER
3364	T145	*TEST CLOCK B'S 1KHZ DIVIDER
3365	T146	*TEST CLOCK B'S 100HZ DIVIDER
3393		
3395		END OF PASS ROUTINE
3396	*	
3397	*	SPECIAL I/O SIGNAL TESTS
3398	*	
3434	*	'STP2 OUT' TO 'SCHMITT TRIG 1 IN' TESTS
3484	;*:	'STP1 OUT' TO 'SCHMITT TRIG 2' H TESTS
3538	*	'SCHMITT TRIG 3' IN, 'ST3 OUT' TESTS
3590	*	'A EVENT OUT' TEST
3643	*	'B EVENT OUT' TEST
3733		
3734		*SYSMAC ROUTINES
3735		
3737		BINARY TO OCTAL (ASCII) AND TYPE
3738		ERROR HANDLER ROUTINE
3739		ERROR MESSAGE TYPEOUT ROUTINE
3740		CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
3741		SCOPE HANDLER ROUTINE
3742		READ AN OCTAL NUMBER FROM THE TTY
3743		TTY INPUT ROUTINE
3744		TYPE ROUTINE
3745		APT COMMUNICATIONS ROUTINE
3746		POWER DOWN AND UP ROUTINES
3751		TRAP DECODER
(3)		TRAP TABLE

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.REM [

CRLPAB.MAC

WELCOME, THIS DIAGNOSTIC IS ONE IN A SERIES OF DIAGNOSTIC
DESIGNED IN ORDER TO AID YOU IN TESTING THE LPA-11XX OPTION.
I HOPE THAT YOU HAVE READ THE DOCUMENTATION SECTION OF THIS
DIAGNOSTIC. IF YOU HAVE, YOU KNOW ABOUT ALL OF THE DIAGNOSTICS
THAT ARE AVAILABLE FOR TESTING THE LPA SYSTEM.

GOOD LUCK !

[
.GLOBL DRLPX2

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.TITLE MMAST.MAC
.IDENT /4.01/
:
: LPA11-K MICRO CODE
:
: CHARLES A. SAMUELSON
: NOVEMBER, 1977
:

.TITLE DMAST.MAC
.IDENT /4.01/
:
: LPA11-K MICRO CODE
:
: CHARLES A. SAMUELSON
: NOVEMBER, 1977
:

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.REM !

THIS IS A LIST OF TESTS DELETED FROM THIS DIAGNOSTIC.
THESE TEST COULD NOT BE DONE THROUGH THE LPA-11.

TEST THE LOW BYTE OPERATION OF CLOCK A'S STATUS REGISTER
TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER
TEST THE LOW BYTE OPERATION OF B'S STATUS REGISTER
TEST THE HIGH BYTE OPERATION OF B'S STATUS REGISTER
TEST THAT INIT CLEARS STATUS REGISTER A
TEST THAT INIT CLEARS BUFFER REGISTER A
TEST THAT INIT CLEARS STATUS REGISTER B
TEST THAT INIT CLEARS BUFFER REGISTER B
TEST THAT A'S COUNT REGISTER IS CLEARED BY INIT
TEST THAT CLOCK A WILL INTR. AND TO THE RIGHT VECTOR
TEST THAT CLOCK A WILL INTR. WHEN CPU PSW = CLK INTR LEV -1
TEST THAT CLOCK A WILL NOT INTR. WHEN CPU PSW = CLK INTR LEVEL
TEST THAT ST1 WILL CAUSE CLOCK A TO INTER.
TEST THAT CLOCK A OVERFLOW WILL CAUSE AN INTR.
TEST THAT A CLOCK A COUNTER BUFFER WILL CAUSES AN INTR.
TEST THAT CLOCK B WILL INTR. AND TO THE RIGHT VECTOR
TEST THAT CLOCK B WILL INTR. WHEN CPU PSW=CLK INTR LEV -1
TEST THAT CLOCK B WILL NOT INTR. WHEN CPU PSW=CLK INTR LEVEL
TEST THAT A CLOCKB OVERFLOW WILL CAUSE AN INTR.
TEST CLOCK A'S REPEATIBILITY AT 1MHZ RATE
TEST CLOCK A'S REPEATIBILITY AT 100KHZ RATE
TEST CLOCK A'S REPEATIBILITY AT 10KHZ RATE
TEST CLOCK A'S REPEATIBILITY AT 1KHZ RATE
TEST CLOCK A'S REPEATIBILITY AT 100HZ RATE
TEST CLOCK B'S REPEATIBILITY AT 1MHZ RATE
TEST CLOCK B'S REPEATIBILITY AT 100KHZ RATE
TEST CLOCK B'S REPEATIBILITY AT 10KHZ RATE
TEST CLOCK B'S REPEATIBILITY AT 1KHZ RATE
TEST CLOCK B'S REPEATIBILITY AT 100HZ RATE
TEST THAT "INIT" CLEARS B'S 100KHZ DIVIDE BY 10 CHIPS

.TITLE LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
;*COPYRIGHT (C) 1980
;*DIGITAL EQUIPMENT CORP.
;*MAYNARD, MASS. 01754
*
;*PROGRAM BY EDWARD C. BADGER REV B BY R. SHOOP
*
;*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
;*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
*
\$TN=1

.SBTTL OPERATIONAL SWITCH SETTINGS
*
* SWITCH USE
*-----
* 15 HALT ON ERROR
* 14 LOOP ON TEST
* 13 INHIBIT ERROR TYPEOUTS

```
(1)
(1)
(1)
1209
(1)
(1)      000000
(1)
(1)
(1)
(1)      000174
(1) 000174 000000
(1) 000176 000000
1210      000200
1211 000200 000137 001726
1212
1213 000204 000137 002462
1214 000210 000137 022450
1215 000214 000137 022646
1216 000220 000137 023062
1217 000224 000137 023246
1218 000230 000137 023454
1219
1220
(1)
(1)
(1)      001100
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(1)
(1)      000011
(1)      000012
(1)      000015
(1)      000200
(1)      177776
(1)
(1)      177774
(1)      177772
(1)      177570
(1)      177570
(1)
(1)
(1)      000000
(1)      000001
(1)      000002
(1)      000003
(1)      000004
(1)      000005
(1)      000006
(1)      000007
(1)      000006
(1)      000007
(1)
(1)
(1)      000000
(1)      000040
```

```
.*      10      BELL ON ERROR
.*      9      LOOP ON ERROR
.*      8      LOOP ON TEST IN SWR<7:0>
.SBTTL TRAP CATCHER

.=0
; *ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
; *SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
; *LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
.=174
DISPREG: .WORD 0      ;;SOFTWARE DISPLAY REGISTER
SWREG:   .WORD 0      ;;SOFTWARE SWITCH REGISTER
.=200
JMP      @#START      ;GO TO STARTING ADDRESS OF PROGRAM
JMP      @#RSTART     ;GO TO RESTART ADDRESS.
JMP      @#LS210      ;GO TO SPECIAL TEST #1.
JMP      @#LS214      ;GO TO SPECIAL TEST #2.
JMP      @#LS220      ;GO TO SPECIAL TEST #3.
JMP      @#LS224      ;GO TO SPECIAL TEST #4.
JMP      @#LS230      ;GO TO SPECIAL TEST #5.

.SBTTL BASIC DEFINITIONS
; *INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
STACK= 1100
.EQUIV  EMT,ERROR     ;;BASIC DEFINITION OF ERROR CALL
.EQUIV  IOT,SCOPE     ;;BASIC DEFINITION OF SCOPE CALL

; *MISCELLANEOUS DEFINITIONS
HT=     11            ;;CODE FOR HORIZONTAL TAB
LF=     12            ;;CODE FOR LINE FEED
CR=     15            ;;CODE FOR CARRIAGE RETURN
CRLF=   200          ;;CODE FOR CARRIAGE RETURN-LINE FEED
PS=     177776       ;;PROCESSOR STATUS WORD
.EQUIV  PS,PSW
STKLMT= 177774       ;;STACK LIMIT REGISTER
PIRQ=   177772       ;;PROGRAM INTERRUPT REQUEST REGISTER
DSWR=   177570       ;;HARDWARE SWITCH REGISTER
DDISP=  177570       ;;HARDWARE DISPLAY REGISTER

; *GENERAL PURPOSE REGISTER DEFINITIONS
R0=     %0           ;;GENERAL REGISTER
R1=     %1           ;;GENERAL REGISTER
R2=     %2           ;;GENERAL REGISTER
R3=     %3           ;;GENERAL REGISTER
R4=     %4           ;;GENERAL REGISTER
R5=     %5           ;;GENERAL REGISTER
R6=     %6           ;;GENERAL REGISTER
R7=     %7           ;;GENERAL REGISTER
SP=     %6           ;;STACK POINTER
PC=     %7           ;;PROGRAM COUNTER

; *PRIORITY LEVEL DEFINITIONS
PR0=    0            ;;PRIORITY LEVEL 0
PR1=    40          ;;PRIORITY LEVEL 1
```



```

(1) .EQUIV BIT05,BIT5
(1) .EQUIV BIT04,BIT4
(1) .EQUIV BIT03,BIT3
(1) .EQUIV BIT02,BIT2
(1) .EQUIV BIT01,BIT1
(1) .EQUIV BIT00,BIT0

(1) ;*BASIC "CPU" TRAP VECTOR ADDRESSES
(1) ERRVEC= 4 ;:TIME OUT AND OTHER ERRORS
(1) RESVEC= 10 ;:RESERVED AND ILLEGAL INSTRUCTIONS
(1) TBITVEC=14 ;: "T" BIT
(1) TRTVEC= 14 ;:TRACE TRAP
(1) BPTVEC= 14 ;:BREAKPOINT TRAP (BPT)
(1) IOTVEC= 20 ;:INPUT/OUTPUT TRAP (IOT) **SCOPE**
(1) PWRVEC= 24 ;:POWER FAIL
(1) EMTVEC= 30 ;:EMULATOR TRAP (EMT) **ERROR**
(1) TRAPVEC=34 ;: "TRAP" TRAP
(1) TKVEC= 60 ;:TTY KEYBOARD VECTOR
(1) TPVEC= 64 ;:TTY PRINTER VECTOR
(1) PIRQVEC=240 ;:PROGRAM INTERRUPT REQUEST VECTOR

1221 170404 ABASE= 170404
1222 000344 AVECT1= 344
1223 000006 APRIOR= 6
1265
1275 .SBTTL ACT11 HOOKS

(1) ;:*****
(2) ;HOOKS REQUIRED BY ACT11
(1) $SVPC= . ;SAVE PC
(1) 000234 .=46
(1) 000046 $ENDAD ;:1)SET LOC.46 TO ADDRESS OF $ENDAD IN .$EOP
(1) 000046 022414
(1) 000052 .=52
(1) 000052 000000 ;:2)SET LOC.52 TO ZERO
(1) 000234 ;: RESTORE PC
(1) 001000 .=1000
1276
1277 .SBTTL APT PARAMETER BLOCK

(1) ;:*****
(2) ;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
(1) ;:*****
(2) ;:*****
(1) 001000 .$X= . ;:SAVE CURRENT LOCATION
(1) 000024 .=24 ;:SET POWER FAIL TO POINT TO START OF PROGRAM
(1) 000024 000200 200 ;:FOR APT START UP
(1) 000044 .=44 ;:POINT TO APT INDIRECT ADDRESS PNTR.
(1) 000044 001000 $APTHDR ;:POINT TO APT HEADER BLOCK
(1) 001000 .=.$X ;:RESET LOCATION COUNTER
(2) ;:*****
(1) ;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
(1) ;INTERFACE SPEC.

(1) $APTHD:
(1) 001000 000000 $SHIBTS: .WORD 0 ;:TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
(1) 001002 001200 $MBADR: .WORD $MAIL ;:ADDRESS OF APT MAILBOX (BITS 0-15)
(1) 001004 000002 $STMT: .WORD 2 ;:RUN TIM OF LONGEST TEST
(1) 001006 000120 $PASTM: .WORD 120 ;:RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
(1) 001010 000120 $UNITM: .WORD 120 ;:ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT

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LPA-KW11K DIAGNOSTIC MD-11-CRLPG-C
CRLPGC.P11 18-AUG-80 09:15

MACY11 30G(1063) 24-OCT-80^{M 2} 09:38 PAGE 3-4
APT PARAMETER BLOCK

SEQ 0025

(1) 001012 000052
1278

.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)

(2)	001210	000000	\$DEVCT:	.WORD	ADEVCT	::DEVICE COUNT
(2)	001212	000000	\$UNIT:	.WORD	AUNIT	::I/O UNIT NUMBER
(2)	001214	000000	\$MSGAD:	.WORD	AMSGAD	::MESSAGE ADDRESS
(2)	001216	000000	\$MSGLG:	.WORD	AMSGLG	::MESSAGE LENGTH
(2)	001220		\$ETABLE:			::APT ENVIRONMENT TABLE
(2)	001220	000	\$ENV:	.BYTE	AENV	::ENVIRONMENT BYTE
(2)	001221	000	\$ENVM:	.BYTE	AENVM	::ENVIRONMENT MODE BITS
(2)	001222	000000	\$SWREG:	.WORD	ASWREG	::APT SWITCH REGISTER
(2)	001224	000000	\$USWR:	.WORD	AUSWR	::USER SWITCHES
(2)	001226	000000	\$CPUOP:	.WORD	ACPUOP	::CPU TYPE,OPTIONS
(2)			*			BITS 15-11=CPU TYPE
(2)			*			11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
(2)			*			11/70=06,PDQ=07,Q=10
(2)			*			BIT 10=REAL TIME CLOCK
(2)			*			BIT 9=FLOATING POINT PROCESSOR
(2)			*			BIT 8=MEMORY MANAGEMENT
(2)	001230	000	\$MAMS1:	.BYTE	AMAMS1	::HIGH ADDRESS,M.S. BYTE
(2)	001231	000	\$MTYP1:	.BYTE	AMTYP1	::MEM. TYPE,BLK#1
(2)			*			MEM.TYPE BYTE -- (HIGH BYTE)
(2)			*			900 NSEC CORE=001
(2)			*			300 NSEC BIPOLAR=002
(2)			*			500 NSEC MOS=003
(2)	001232	000000	\$MADR1:	.WORD	AMADR1	::HIGH ADDRESS,BLK#1
(2)			*			MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF 'TYPE' ABOVE
(2)	001234	000	\$MAMS2:	.BYTE	AMAMS2	::HIGH ADDRESS,M.S. BYTE
(2)	001235	000	\$MTYP2:	.BYTE	AMTYP2	::MEM. TYPE,BLK#2
(2)	001236	000000	\$MADR2:	.WORD	AMADR2	::MEM.LAST ADDRESS,BLK#2
(2)	001240	000	\$MAMS3:	.BYTE	AMAMS3	::HIGH ADDRESS,M.S.BYTE
(2)	001241	000	\$MTYP3:	.BYTE	AMTYP3	::MEM. TYPE,BLK#3
(2)	001242	000000	\$MADR3:	.WORD	AMADR3	::MEM.LAST ADDRESS,BLK#3
(2)	001244	000	\$MAMS4:	.BYTE	AMAMS4	::HIGH ADDRESS,M.S.BYTE
(2)	001245	000	\$MTYP4:	.BYTE	AMTYP4	::MEM. TYPE,BLK#4
(2)	001246	000000	\$MADR4:	.WORD	AMADR4	::MEM.LAST ADDRESS,BLK#4
(2)	001250	000344	\$VECT1:	.WORD	AVECT1	::INTERRUPT VECTOR#1,BUS PRIORITY#1
(2)	001252	000000	\$VECT2:	.WORD	AVECT2	::INTERRUPT VECTOR#2BUS PRIORITY#2
(2)	001254	170404	\$BASE:	.WORD	ABASE	::BASE ADDRESS OF EQUIPMENT UNDER TEST
(2)	001256	000000	\$DEVN:	.WORD	ADEVN	::DEVICE MAP
(2)	001260	000000	\$CDW1:	.WORD	ACDW1	::CONTROLLER DESCRIPTION WORD#1
(2)	001262	000000	\$CDW2:	.WORD	ACDW2	::CONTROLLER DESCRIPTION WORD#2
(2)	001264	000000	\$DDW0:	.WORD	ADDW0	::DEVICE DESCRIPTOR WORD#0
(2)	001266	000000	\$DDW1:	.WORD	ADDW1	::DEVICE DESCRIPTOR WORD#1
(2)	001270	000000	\$DDW2:	.WORD	ADDW2	::DEVICE DESCRIPTOR WORD#2
(2)	001272	000000	\$DDW3:	.WORD	ADDW3	::DEVICE DESCRIPTOR WORD#3
(2)	001274	000000	\$DDW4:	.WORD	ADDW4	::DEVICE DESCRIPTOR WORD#4
(2)	001276	000000	\$DDW5:	.WORD	ADDW5	::DEVICE DESCRIPTOR WORD#5
(2)	001300	000000	\$DDW6:	.WORD	ADDW6	::DEVICE DESCRIPTOR WORD#6
(2)	001302	000000	\$DDW7:	.WORD	ADDW7	::DEVICE DESCRIPTOR WORD#7
(2)	001304	000000	\$DDW8:	.WORD	ADDW8	::DEVICE DESCRIPTOR WORD#8
(2)	001306	000000	\$DDW9:	.WORD	ADDW9	::DEVICE DESCRIPTOR WORD#9
(2)	001310	000000	\$DDW10:	.WORD	ADDW10	::DEVICE DESCRIPTOR WORD#10
(2)	001312	000000	\$DDW11:	.WORD	ADDW11	::DEVICE DESCRIPTOR WORD#11
(2)	001314	000000	\$DDW12:	.WORD	ADDW12	::DEVICE DESCRIPTOR WORD#12
(2)	001316	000000	\$DDW13:	.WORD	ADDW13	::DEVICE DESCRIPTOR WORD#13
(2)	001320	000000	\$DDW14:	.WORD	ADDW14	::DEVICE DESCRIPTOR WORD#14
(2)	001322	000000	\$DDW15:	.WORD	ADDW15	::DEVICE DESCRIPTOR WORD#15

(2)
(2) 001324
(2)
(3)
(3) 001324 170404
(3) 001326 170406
(3) 001330 170430
(3)
(3) 001332 170432
(3) 001334 170434
(3) 001336 170436
(3)
(3) 001340 000344
(3) 001342 000346
(3)
(3) 001344 000364
(3) 001346 000366
(3)
(3) 001350 000006
(3) 001352 000006
(3) 001354 000000
(3)
(3)

\$ETEND:

ASR: 170404 ;/CLOCK A STATUS REGISTER.
ABR: 170406 ;/CLOCK A BUFFER REGISTER.
ACR: 170430 ;/CLOCK A COUNT REGISTER.

BSR: 170432 ;/CLOCK B STATUS REGISTER.
BBR: 170434 ;/CLOCK B BUFFER REGISTER.
BCR: 170436 ;/CLOCK B COUNT REGISTER.

AVECT: 344 ;/CLOCK A INTR. VECTOR ADDR.
AVECP2: 346 ;/CLOCK A INTR. STATUS WORD.

BVECT: 364 ;/CLOCK B INTR. VECTOR ADDR.
BVECT2: 366 ;/CLOCK B INTR. STATUS WORD.

APRITY: 6 ;/PRIORITY LEVEL OF CLOCK A.
BPRITY: 6 ;/PRIORITY LEVEL OF CLOCK B.
\$TMDAT: 0

1320			:ITEM 6		
1321					
1322	001426	027355	EM6	:CLOCK B BR DATA ERROR	
1323	001430	030243	DH6	:ERRPC BBR WAS S/B	
1324	001432	030736	DT6	:\$ERRPC, BBR, \$BDDAT, \$GDDAT	
1325	001434	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1326					
1327			:ITEM 7		
1328					
1329	001436	027404	EM7	:CLOCK B CR DATA ERROR	
1330	001440	030301	DH7	:ERRPC BCR WAS S/B	
1331	001442	030750	DT7	:\$ERRPC, BCR, \$BDDAT, \$GDDAT	
1332	001444	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1333					
1334			:ITEM 10		
1335					
1336	001446	027433	EM10	:DUAL ADDRESS ERROR	
1337	001450	030337	DH10	:ERROR GOOD BAD GOOD DATA READ FROM	
1338				: PC ADDR ADDR DATA DUAL ADDRESS	
1339	001452	030762	DT10	:\$ERRPC, \$GDADR, \$BDADR, \$GDDAT, \$BDDAT	
1340	001454	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1341					
1342			:ITEM 11		
1343					
1344	001456	027460	EM11	:CLOCK A COUNT ERROR	
1345	001460	030147	DH4	:ERRPC ACR WAS S/B	
1346	001462	030712	DT4	:\$ERRPC, ACR, \$BDDAT, \$GDDAT	
1347	001464	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1348					
1349			:ITEM 12		
1350					
1351	001466	027507	EM12	:CLOCK A COUNT FUNCTION ERROR	
1352	001470	030476	DH12	:ERRPC ASR	
1353	001472	030776	DT12	:ERRPC, ASR	
1354	001474	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1355					
1356			:ITEM 13		
1357					
1358	001476	031070	DF0	:ERROR 13 DOES NOT EXIST.	
1359	001500	031070	DF0	:IT WOULD BE BAD LUCK.	
1360	001502	031070	DF0		
1361	001504	031070	DF0		
1362					
1363			:ITEM 14		
1364					
1365	001506	027547	EM14	:CLOCK B COUNT FUNCTION ERROR	
1366	001510	030515	DH14	:ERRPC BSR	
1367	001512	031004	DT14	:\$ERRPC, BSR	
1368	001514	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM	
(1)					
1369					

1370				
1371				
1372	001516	027607	EM15	:CLOCK B COUNT ERROR
1373	001520	030301	DH7	:ERRPC CSR WAS S/B
1374	001522	030750	DT7	:\$ERRPC, BCR, \$BDDAT, \$GDDAT
1375	001524	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1376				
1377				
1378				
1379	001526	027636	EM16	:CLOCK A INTERRUPT ERROR
1380	001530	030476	DH12	:ERRPC ASR
1381	001532	030776	DT12	:\$ERRPC, ASR
1382	001534	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1383				
1384				
1385				
1386	001536	027671	EM17	:CLOCK B INTERRUPT ERROR
1387	001540	030515	DH14	:ERRPC BSR
1388	001542	031004	DT14	:\$ERRPC, BSR
1389	001544	031070	DF0	
1390				
1391				
1392				
1393	001546	027724	EM20	:CLOCK A REPEATABILITY ERROR
1394	001550	030533	DH20	:ERROR ASR 2ND CNT 1ST CNT
1395	001552	030666	DT1	:\$ERRPC, ASR, \$BDDAT, \$GDDAT
1396	001554	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1397				
1398				
1399				
1400	001556	027460	EM11	:CLOCK A COUNT ERROR
1401	001560	030147	DH4	:ERROR ASR 2ND CNT 1ST CNT
1402	001562	031012	DT21	:\$ERRPC, ASR, \$BDDAT, \$GDDAT
1403	001564	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1404				
1405				
1406				
1407	001566	027460	EM11	:CLOCK A COUNT ERROR
1408	001570	030147	DH4	:ERRPC ASR WAS S/B
1409	001572	031024	DT22	:\$ERRPC, ACR, \$BDDAT, \$TMPO
1410	001574	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1411				
1412				
1413				
1414	001576	027763	EM23	:CLOCK B REPEATABILITY ERROR
1415	001600	030575	DH23	:ERROR ASR 2NDCNT 1STCNT
1416	001602	030666	DT1	:\$ERRPC, ASR, \$BDDAT, \$GDDAT
1417	001604	031070	DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)				
1418				
1419				

1420					
1421	001606	027607	EM15		:CLOCK B COUNT ERROR
1422	001610	030301	DH7		:ERRPC BCR WAS S/B
1423	001612	031036	DT24		:\$ERRPC,BCR,\$GDDAT,\$TMPO
1424	001614	031070	DF0		:ALL NUMBERS ARE IN OCTAL FORM
(1)					
1425					
1426			:ITEM	25	
1427					
1428	001616	027607	EM15		:CLOCK B COUNT ERROR
1429	001620	030301	DH7		:ERRPC BCR WAS S/B
1430	001622	031050	DT25		:\$ERRPC,BCR,\$BDDAT,\$TMPO
1431	001624	031070	DF0		:ALL NUMBERS ARE IN OCTAL FORM
(1)					
1432					
1433			:ITEM	26	
1434					
1435	001626	030022	EM26		:CLOCK ADDRESSING ERROR
1436	001630	030637	DH26		:ERRPC CLOCK ADDR.
1437	001632	031062	DT26		:\$ERRPC,\$TMPO
1438	001634	031070	DF0		:ALL NUMBERS ARE IN OCTAL FORM
(1)					
1439					
(1)			:		:ADDRESS OF KMC-11 OF LPA-11
(1)			:		THE ADDR FOR KMADO MAY BE
(1)			:		CHANGED BY THE USER TO REFLECT
(1)			:		A DIFFERENT KMC-11 ADDR. THE
(1)			:		REST OF THE ADDRESSES WILL
(1)			:		BE CHANGED BY THE PROGRAM.
(1)			:		
(1)	001636		LPCI:		
(1)	001636	170460	KMADO:	.WORD 170460	:BASE KMC ADDR. MAY BE PATCHED BY USER.
(1)					
(1)	001640		LPMR:		
(1)	001640	170461	KMAD1:	.WORD 170460+1	;>DO NOT <;KMC-CSR ADDR
(1)	001642		LPCO:		
(1)	001642	170462	KMAD2:	.WORD 170460+2	;>PATCH <;
(1)	001644		LPSO:		
(1)	001644	170463	KMAD3:	.WORD 170460+3	;>THIS AREA <
(1)	001646		LPADL:		
(1)	001646	170464	KMAD4:	.WORD 170460+4	:
(1)	001650		LPADH:		
(1)	001650	170465	KMAD5:	.WORD 170460+5	;>DO NOT <
(1)	001652		LPMS1:		
(1)	001652	170466	KMAD6:	.WORD 170460+6	;>PATCH <
(1)	001654		LPMS2:		
(1)	001654	170467	KMAD7:	.WORD 170460+7	;>THIS AREA <
(1)					
(1)	001656	000344	VECTOR:	.WORD AVECT18777	:BASE VECTOR OF KMC
(1)	001660	000350	VECTPS:	.WORD 4+AVECT18777	:VECTR ADDR.+2
(1)					
(1)	001662	000005	VERSN:	.WORD 5	:CURRENT VERSION NUMBER OF MICROCODE.
(1)					
(1)	001664	000000	.DVLS:	.WORD 0	;/DEVICE LIST OF I/O ADDR. DEFINED
(1)	001666	000020	.BLKW	16.	;/BY INIT.
(1)					

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CRLPGC.P11 18-AUG-80 09:15

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PROGRAM START

SEQ 0033

1440

.SBTTL PROGRAM START

1443
 1444 001726
 (1)
 (1)
 (1) 001726 012706 001100
 (1) 001732 005026
 (1) 001734 022706 001140
 (1) 001740 001374
 (1) 001742 012706 001100
 (1)
 (1) 001746 012737 025062 000020
 (1) 001754 012737 000340 000022
 (1) 001762 012737 024302 000030
 (1) 001770 012737 000340 000032
 (1) 001776 012737 027102 000034
 (1) 002004 012737 000340 000036
 (1) 002012 012737 026662 000024
 (1) 002020 012737 000340 000026
 (1) 002026 013737 022362 022354
 (1) 002034 005037 001166
 (1) 002040 112737 000001 001115
 (1) 002046 012737 002046 001106
 (1) 002054 012737 002054 001110
 (2)
 (2)
 (2) 002062 013746 000004
 (2) 002066 012737 002122 000004
 (2) 002074 012737 177570 001140
 (2) 002102 012737 177570 001142
 (2) 002110 022777 177777 177022
 (2) 002116 001012
 (2)
 (2) 002120 000403
 (2) 002122 012716 002130
 (2) 002126 000002
 (2) 002130 012737 000176 001140
 (2) 002136 012737 000174 001142
 (2) 002144 012637 000004
 (1)
 (2) 002150 005037 001206
 (2) 002154 132737 000200 001221
 (2) 002162 001403
 (2) 002164 012737 001222 001140
 (2) 002172
 1445 002172 122737 000001 001134
 1446 002200 001426
 1447
 1448 002202 104401 002210
 (1) 002206 000423
 (1)
 (1) 002256
 1449
 1450 002256 013737 001254 001324
 1451 002264 012737 000001 001210
 1452 002272 005037 001206
 1453

START:
 .SBTTL INITIALIZE THE COMMON TAGS
 ;;CLEAR THE COMMON TAGS (\$CMTAG) AREA
 MOV #CMTAG,R6 ;;FIRST LOCATION TO BE CLEARED
 CLR (R6)+ ;;CLEAR MEMORY LOCATION
 CMP #SWR,R6 ;;DONE?
 BNE -6 ;;LOOP BACK IF NO
 MOV #STACK,SP ;;SETUP THE STACK POINTER
 ;;INITIALIZE A FEW VECTORS
 MOV #SCOPE,@IOTVEC ;;IOT VECTOR FOR SCOPE ROUTINE
 MOV #340,@IOTVEC+2 ;;LEVEL 7
 MOV #ERROR,@EMTVEC ;;EMT VECTOR FOR ERROR ROUTINE
 MOV #340,@EMTVEC+2 ;;LEVEL 7
 MOV #STRAP,@TRAPVEC ;;TRAP VECTOR FOR TRAP CALLS
 MOV #340,@TRAPVEC+2;LEVEL 7
 MOV #SPWRDN,@PWRVEC ;;POWER FAILURE VECTOR
 MOV #340,@PWRVEC+2 ;;LEVEL 7
 MOV \$ENDCT,\$EOPCT ;;SETUP END-OF-PROGRAM COUNTER
 CLR \$ESCAPE ;;CLEAR THE ESCAPE ON ERROR ADDRESS
 MOVB #1,\$ERMAX ;;ALLOW ONE ERROR PER TEST
 MOV #,\$SLPADR ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
 MOV #,\$SLPERR ;;SETUP THE ERROR LOOP ADDRESS
 ;;SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
 ;;EQUAL TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.
 MOV @ERRVEC,-(SP) ;;SAVE ERROR VECTOR
 MOV #64\$,@ERRVEC ;;SET UP ERROR VECTOR
 MOV #DSWR,SWR ;;SETUP FOR A HARDWARE SWICH REGISTER
 MOV #DDISP,DISPLAY ;;AND A HARDWARE DISPLAY REGISTER
 CMP #-1,@SWR ;;TRY TO REFERENCE HARDWARE SWR
 BNE 66\$;;BRANCH IF NO TIMEOUT TRAP OCCURRED
 ;;AND THE HARDWARE SWR IS NOT = -1
 BR 65\$;;BRANCH IF NO TIMEOUT
 64\$: MOV #65\$,(SP) ;;SET UP FOR TRAP RETURN
 RTI
 65\$: MOV #SWREG,SWR ;;POINT TO SOFTWARE SWR
 MOV #DISPREG,DISPLAY
 66\$: MOV (SP)+,@ERRVEC ;;RESTORE ERROR VECTOR
 CLR \$PASS ;;CLEAR PASS COUNT
 BITB #APTSIZE,\$ENVM ;;TEST USER SIZE UNDER APT
 BEQ 67\$;;YES,USE NON-APT SWITCH
 MOV #SSWREG,SWR ;;NO,USE APT SWITCH REGISTER
 67\$: CMPB #1,\$AUTOB ;IF RUNNING XXDP ETC.
 BEQ 10\$
 TYPE ,69\$;;TYPE ASCIZ STRING
 BR 68\$;;GET OVER THE ASCIZ
 ;;69\$: .ASCIZ <15><12><12>#CRLPGC LPA/KW11-K DIAGNOSTIC#<15><12>
 68\$:
 10\$: MOV \$BASE,ASR
 MOV #1,\$DEVCT
 CLR \$PASS

```

1454
(1)
(1)
(1)
(1) 002276 010046
(1) 002300 010146
(1) 002302 013700 001636
(1) 002306 012701 001640
(1)
(1) 002312 005200
(1) 002314 010021
(1) 002316 020127 001656
(1) 002322 001373
(1) 002324 005037 001664
(1) 002330 012601
(1) 002332 012600
1455
1456 002334
1457 002334 005000
1458 002336 005200
1459 002340 001376
1460 002342 013700 001324
1461 002346 062700 000002
1462 002352 010037 001326
1463 002356 062700 000022
1464 002362 010037 001330
1465 002366 062700 000002
1466 002372 010037 001332
1467 002376 062700 000002
1468 002402 010037 001334
1469 002406 062700 000002
1470 002412 010037 001336
1471
1472 002416 013700 001340
1473 002422 062700 000002
1474 002426 010037 001342
1475 002432 062700 000016
1476 002436 010037 001344
1477 002442 062700 000002
1478 002446 010037 001346
1479
1480 002452 013737 001350 001352
1481 002460 000402
1482 002462 005037 001664
1483 002466 012706 001100
1484 002472 012746 000340
1485 002476 012746 002504
1486 002502 000002
1487 002504
1488
1489
1490
1491

; THIS SECTION OF CODE HANDLES INITIALIZING LPA-11 FUNCTIONS
;
MOV R0,-(SP)
MOV R1,-(SP)
MOV KMADO,R0 ;GET KMC-11 ADDRESS.
MOV #KMAD1,R1 ;GET ADDR. OF ADDR. LIST.
70$: INC R0 ;UPDATE ADDR.
MOV R0,(1)+ ;WRITE ADDR.
CMP R1,#KMAD7+2 ;DONE ALL ADDRESSES?
BNE 70$ ;NO - DO NEXT ADDR.
CLR .DVLS ;CLR ADDR. LIST.
MOV (SP)+,R1
MOV (SP)+,R0
LOOP:
CLR R0
1$: INC R0 ;DELAY SOME TIME SO THAT FIRST RESET
BNE 1$ ;INSTR. WON'T CLOBBER TYPEOUT.
MOV ASR,R0 ;NOW WE'RE GONNA FIX
ADD #2,R0 ;ALL CLOCK ADDRESSES BASED ON ASR.
MOV R0,ABR
ADD #22,R0
MOV R0,ACR
ADD #2,R0
MOV R0,BSR
ADD #2,R0
MOV R0,BBR
ADD #2,R0
MOV R0,BCR
MOV AVECT,R0 ;NOW FIX VECTOR ADDRESSES
ADD #2,R0 ;BASED ON AVECT.
MOV R0,AVECP2
ADD #16,R0
MOV R0,BVECT
ADD #2,R0
MOV R0,BVECT2
MOV APRITY,BPRITY ;FIX CLK B'S PRIORITY BASED ON A'S.
BR SSTART
RSTART: CLR .DVLS
SSTART: MOV #STACK,SP
MOV #340,-(SP) ;SET PROCESSOR PRIORITY TO 7.
MOV #1$,-(SP)
RTI
1$:
.SBTTL *
.SBTTL * PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
.SBTTL *

```

1518
(1)
(5)
(4)
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(4)

002504	000240		
002506	112737	000001	001102
002514	112737	000001	001204

```
*****
*TEST 1          *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
*
*'BUS A17': 'A04'='DEVICE' H; 'DEVICE' H + 'TPO' H='DEV ENABLE' H
*'DEV ENABLE' H+'TP1' H='DEV ENB 2' H
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17'
*
* CLOCK ADDRESS TEST. SCOPE FOR 'DEV ENB Z' H AND WORK BACK
*
*****
TST1:  NOP
1$:   MOVB  #1,$TSTNM
      MOVB  #1,$TESTN
*
*      MOV   @ASR,$BDDAT    ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
*      MOV   @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
*      MOV   @ACR,$BDDAT    ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
*      MOV   @BSR,$BDDAT    ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
*      MOV   @BBR,$BDDAT    ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
*      MOV   @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
*
*****
*TEST 2          *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
*
*FOR LOADING DATA:
*
*(WE KNOW WE CAN ADDR. KW11), 'BUS A01' L + 'A02' H + 'A03' H
*+'BUS C1' L='LD BUFF A' L
*LD BUF A' L + BUFFERED DATA LOADS INTO MUX LATCH (NOTE WE KNOW
*BY NOW 'TP1' L SHOULD BE GOOD).
*
* FOR READING DATA:
*
*BUS A01 L + (DATA 1N H + EV ENABLE(1) H)=RD BUFF AL
*[BA01H*(DEPENDING ON WHICH DATA BITS READ) RD BUF AL]+BUFF A00:15
* +[DEV ENABLE*DATA IN L]=BUS DATA
*
*
*SINCE WE WONT LOOK FOR ANY SPECIFIC DATA BIT FAILURE,
*JUST THAT WE CAN WRITE INTO BUFFER + READ BACK,
*IF FAILED, KEY ON 'LD BUFF A L' AND 'RD BUFF A L'
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'BUS A17' (2 OCCURANCES PER LOOP)
*
*****
```


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(3)
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1581

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1584

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1586
1603
1604
(3)
(4)
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(4)
(3)

002642 000004

```
:::*****  
TST3:  SCOPE
```

002644 005037 001124

```
CLR  $GDDAT      ;INDICATE WE EXPECT 0'S.  
          ;CLEAR BUFFER REGISTER.  
          ;READ CLOCK A'S BUFFER REGISTER
```

```
;*  MOV  $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
;*  MOV  @ABR,$BDDAT      ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
TST  $GDDAT  
BEQ  1$               ;SHOULD BE CLEAR - IF CLEAR - NEXT TEST.
```

002670 005737 001126
002674 001401

```
:::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

002676 104003

```
ERROR 3          ;CLEAR INTR. FAILED TO CLEAR CLOCK A'S  
                ;BUFFER REGISTER.
```

```
:::$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

002700

1\$:

```
:::*****  
*TEST 4          *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ  
*  
*NOW THAT WE CAN WRITE INTO THE BUFFER REGISTER, WE'RE GOING TO TRY  
*WRITING INTO THE STATUS REGISTER AND READ IT BACK.  
*  
*NEW SIGNALS: ['BA03' L + 'BA02' L + 'BA01' L]='LD STAT A' L  
*              'DATA OUT LO' L + 'DATA OUT HI' L + 'LD STATA' L = 'LD STAT A HI' H  
*              + 'LD STATA LO H'  
*FOR READ BACK: 'RD STATA' L  
*  
*NO ATTEMPT MADE TO VERIFY THAT CORRECT DATA CAME BACK, BUT  
*JUST THAT SOME DATA CAME BACK.  
*  
*PROBABLE SYNC POINT FOR THIS TEST:: 'DEV ENABLE (1)' 2 OCCURANCES PER PASS  
*  
*  
:::*****
```



```
(2)                                     :/N
(6) :*****
(5) :*TEST 10      *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(6) :*
(6) :*CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) :*F/FS OR GATES
(7) :*
(7) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) :*
(6) :*
(5) :*****
(4) 003154 000004 TST10: SCOPE
(2)                                     ;/CLEAR THE STATUS REGISTER.
(2)                                     ;/SET BIT 14.
(2)                                     ;/SET FOR ERROR TYPEOUT S/B.
(2)                                     ;/READ THE STATUS REGISTER.
(2) 003156 012737 040000 001124      MOV    #BIT14,$GDDAT
(3)                                     ;*   MOV    $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*   MOV    @ASR,$BDDAT     ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003204 023737 001124 001126      CMP    $GDDAT,$BDDAT     ;/DID BIT 14 AND ONLY BIT 14 SET?
(2) 003212 001402                      BEQ    1$                ;/IF SO-LETS TRY CLEARING IT.
(3)                                     ;:;*****>> ERROR <<*****
(2) 003214 104002                      ERROR  2                ;/ERROR CLOCK AS STATUS REGISTER.
(2)                                     ;/BIT 14 FAILED TO BIT SET.
(3)                                     ;:;*****>> ERROR <<*****
(2) 003216 000416                      BR     2$                ;/BR TO END SUBTEST.
(2) 003220 005037 001124      1$:  CLR    $GDDAT         ;/TRY CLEARING BIT 14.
(2)                                     ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2)                                     ;/NOW READ IT BACK.
(3)                                     ;*   MOV    $GDDAT,@ASR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3)                                     ;*   MOV    @ASR,$BDDAT     ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003244 005737 001126      TST    $BDDAT
(2) 003250 001401                      BEQ    2$                ;/IF ZERO-NO ERROR!
(3)                                     ;:;*****>> ERROR <<*****
(2) 003252 104002                      ERROR  2                ;/ERROR-CLOCK A STATUS REGISTER.
(2)                                     ;/BIT 14 FAILED TO CLEAR.
(3)                                     ;:;*****>> ERROR <<*****
(2) 003254                      2$:
```

```
(2) ;/M
(6) :*****
(5) *TEST 11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
(6) *
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) *
(7) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) *
(6) *
(5) :*****
(4) 003254 000004 TST11: SCOPE
(2) ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 13.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 003256 012737 020000 001124 MOV #BIT13,$GDDAT
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003304 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 13 AND ONLY BIT 13 SET?
(2) 003312 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3)
:::*****>> ERROR <<*****
(2) 003314 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 13 FAILED TO BIT SET.
(3)
:::*****>> ERROR <<*****
(2) 003316 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 003320 1$: ;/TRY CLEARING BIT 13.
(2) 003320 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 003344 005737 001126 TST $BDDAT
(2) 003350 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(3)
:::*****>> ERROR <<*****
(2) 003352 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 13 FAILED TO CLEAR.
(3)
:::*****>> ERROR <<*****
(2) 003354 2$:
```



```
(2)                               :/#  
(6)                               :*****  
(5) *TEST 15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED  
(6)                               :*  
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(6) *F/FS OR GATES  
(7)                               :*  
(7) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(7)                               :*  
(6)                               :*  
(5)                               :*****  
(4) 003654 000004 TST15: SCOPE  
(2)                               :/CLEAR THE STATUS REGISTER.  
(2)                               :/SET BIT 6.  
(2)                               :/SET FOR ERROR TYPEOUT S/B.  
(2)                               :/READ THE STATUS REGISTER.  
(2) 003656 012737 000100 001124 MOV #BIT6,$GDDAT  
(3)                               :/  
(3) * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3)                               :/  
(3) * MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 003704 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?  
(2) 003712 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(3)                               :/  
:::*****>> ERROR <<*****  
(2) 003714 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.  
(2)                               :/BIT 6 FAILED TO BIT SET.  
(3)                               :/  
:::*****>> ERROR <<*****  
(2) 003716 000416 BR 2$ ;/BR TO END SUBTEST.  
(2) 003720 1$: ;/TRY CLEARING BIT 6.  
(2) 003720 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(2)                               :/NOW READ IT BACK.  
(3)                               :/  
(3) * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
(3)                               :/  
(3) * MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
(2) 003744 005737 001126 TST $BDDAT  
(2) 003750 001401 BEQ 2$ ;/IF ZERO-NO ERROR!  
(3)                               :/  
:::*****>> ERROR <<*****  
(2) 003752 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.  
(2)                               :/BIT 6 FAILED TO CLEAR.  
(3)                               :/  
:::*****>> ERROR <<*****  
(2) 003754 2$:
```



```
(2) ;/#
(6) *****
(5) *TEST 17 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(6) *
(6) *CLOCK A STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(6) *F/FS OR GATES
(7) *
(7) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(7) *
(6) *
(5) *****
(4) 004054 000004 TST17: SCOPE
(2) ;/CLEAR THE STATUS REGISTER.
(2) ;/SET BIT 3.
(2) ;/SET FOR ERROR TYPEOUT S/B.
(2) ;/READ THE STATUS REGISTER.
(2) 004056 012737 000010 001124 MOV #BIT3,$GDDAT
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004104 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(2) 004112 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(2) 004114 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER.
(2) ;/BIT 3 FAILED TO BIT SET.
(3) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(2) 004116 000416 BR 2$ ;/BR TO END SUBTEST.
(2) 004120 1$: ;/TRY CLEARING BIT 3.
(2) 004120 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(2) ;/NOW READ IT BACK.
(3) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
(3) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
(2) 004144 005737 001126 TST $BDDAT
(2) 004150 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(3) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(2) 004152 104002 ERROR 2 ;/ERROR-CLOCK A STATUS REGISTER.
(2) ;/BIT 3 FAILED TO CLEAR.
(3) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(2) 004154 2$:
```



```
(3) :
(7) :
(6) :*****:/#
(7) :*TEST 23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 004454 000004 TST23: SCQPE
(3) :/CLEAR THE BUFFER REGISTER.
(3) :/SET BIT 0.
(3) :/SET FOR ERROR TYPEOUT S/B.
(3) :/READ THE BUFFER REGISTER.
(3) 004456 012737 000001 001124 MOV #BIT0,$GDDAT
(4) :* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004504 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 0 AND ONLY BIT 0 SET?
(3) 004512 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(3) :;:*****>> ERROR <<*****
(3) 004514 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) :/BIT 0 FAILED TO BIT SET.
(4)
(3) :;:*****>> ERROR <<*****
(3) 004516 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 004520 1$: ;/TRY CLEARING BIT 0.
(3) 004520 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4) :/NOW READ IT BACK.
(4) :* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) :* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004544 005737 001126 TST $BDDAT
(3) 004550 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(3) :;:*****>> ERROR <<*****
(3) 004552 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) :/BIT 0 FAILED TO CLEAR.
(4)
(3) :;:*****>> ERROR <<*****
(3) 004554 2$:
```



```
(3)                                     :/#
(7) :*****
(6) *TEST 24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 004554 000004 TST24: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 1.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 004556 012737 000002 001124 MOV #BIT1,$GDDAT
(4)                                     :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) :* MOV $GDDAT,@ABR
(4)                                     :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(4) :* MOV @ABR,$BDDAT
(3) 004604 023737 001124 001126 CMP $GDDAT,$BDDAT :/DID BIT 1 AND ONLY BIT 1 SET?
(3) 004612 001402 BEQ 1$ :/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::*****>> ERROR <<*****
(3) 004614 104003 ERROR 3 :/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     :/BIT 1 FAILED TO BIT SET.
(4)
(4) :::*****>> ERROR <<*****
(3) 004616 000416 BR 2$ :/BR TO END SUBTEST.
(3) 004620 1$: :/TRY CLEARING BIT 1.
(3) 004620 005037 001124 CLR $GDDAT :/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     :/NOW READ IT BACK.
(4)
(4) :* MOV $GDDAT,@ABR :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)
(4) :* MOV @ABR,$BDDAT :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004644 005737 001126 TST $BDDAT
(3) 004650 001401 BEQ 2$ :/IF ZERO-NO ERROR!
(4)
(4) :::*****>> ERROR <<*****
(3) 004652 104003 ERROR 3 :/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     :/BIT 1 FAILED TO CLEAR.
(4)
(4) :::*****>> ERROR <<*****
(3) 004654 2$:
```

```

(3)                               ;/#
(7)                               ;*****
(6)                               ;*TEST 25      *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
(7)                               ;*
(7)                               ;*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7)                               ;*F/FS OR GATES
(8)                               ;*
(8)                               ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8)                               ;*
(7)                               ;*
(6)                               ;*****
(5) 004654 000004                 TST25: SCOPE
(3)                               ;/CLEAR THE BUFFER REGISTER.
(3)                               ;/SET BIT 2.
(3)                               ;/SET FOR ERROR TYPEOUT S/B.
(3)                               ;/READ THE BUFFER REGISTER.
(3) 004656 012737 000004 001124      MOV      #BIT2,$GDDAT
(4)                               ;*
(4)                               ;* MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                               ;*
(4)                               ;* MOV      @ABR,$BDDAT    ;/READ DEVICE REG ABK,PUT DATA IN $BDDAT.
(3) 004704 023737 001124 001126      CMP      $GDDAT,$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(3) 004712 001402                    BEQ      1$           ;/IF SO-LETS TRY CLEARING IT.
(4)                               ;;:#####>> ERROR <<#####
(3) 004714 104003                    ERROR    3           ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                               ;/BIT 2 FAILED TO BIT SET.
(4)                               ;;:#####>> ERROR <<#####
(3) 004716 000416                    BR       2$           ;/BR TO END SUBTEST.
(5) 004720                             1$:          ;/TRY CLEARING BIT 2.
(3) 004720 005037 001124            CLR      $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                               ;/NOW READ IT BACK.
(4)                               ;*
(4)                               ;* MOV      $GDDAT,@ABR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                               ;*
(4)                               ;* MOV      @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 004744 005737 001126            TST      $BDDAT
(3) 004750 001401                    BEQ      2$           ;/IF ZERO-NO ERROR!
(4)                               ;;:#####>> FRORR <<#####
(3) 004752 104003                    ERROR    3           ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                               ;/BIT 2 FAILED TO CLEAR.
(4)                               ;;:#####>> ERROR <<#####
(3) 004754                          2$:
    
```



```
(3)                                     :/N
(7) :*****
(6) :*TEST 27      *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 005054 000004 TST27: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 4.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 005056 012737 000020 001124      MOV    #BIT4,$GDDAT
(4)                                     :/
(4) :*      MOV    $GDDAT,@ABR          :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) :*      MOV    @ABR,$BDDAT         :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005104 023737 001124 001126      CMP    $GDDAT,$BDDAT          :/DID BIT 4 AND ONLY BIT 4 SET?
(3) 005112 001402                      BEQ    1$                     :/IF SO-LETS TRY CLEARING IT.
(4)                                     :/
:::*****>> ERROR <<*****
(3) 005114 104003                      ERROR 3                       :/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     :/BIT 4 FAILED TO BIT SET.
(4)                                     :/
:::*****>> ERROR <<*****
(3) 005116 000416                      BR     2$                       :/BR TO END SUBTEST.
(3) 005120 005037 001124      1$:  CLR    $GDDAT                :/TRY CLEARING BIT 4.
(3)                                     :/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     :/NOW READ IT BACK.
(4) :*      MOV    $GDDAT,@ABR          :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) :*      MOV    @ABR,$BDDAT         :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005144 005737 001126      TST    $BDDAT
(3) 005150 001401                      BEQ    2$                       :/IF ZERO-NO ERROR!
(4)                                     :/
:::*****>> ERROR <<*****
(3) 005152 104003                      ERROR 3                       :/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     :/BIT 4 FAILED TO CLEAR.
(4)                                     :/
:::*****>> ERROR <<*****
(3) 005154                      2$:
```

(3) :/ #
(7) :*****
(6) *TEST 30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****

```
(5) 005154 000004 TST30: SCOPE  
(3) ;/CLEAR THE BUFFER REGISTER.  
(3) ;/SET BIT 5.  
(3) ;/SET FOR ERROR TIMEOUT S/B.  
(3) ;/READ THE BUFFER REGISTER.  
(3) 005156 012737 000040 001124 MOV #BITS,$GDDAT  
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
(3) 005204 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?  
(3) 005212 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(4)
```

:::*****>> ERROR <<*****

```
(3) 005214 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.  
(3) ;/BIT 5 FAILED TO BIT SET.  
(4)
```

:::*****>> ERROR <<*****

```
(3) 005216 000416 BR 2$ ;/BR TO END SUBTEST.  
(5) 005220 1$: ;/TRY CLEARING BIT 5.  
(3) 005220 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TIMEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
(3) 005244 005737 001126 TST $BDDAT  
(3) 005250 001401 BEQ 2$ ;/IF ZERO-NO ERROR!  
(4)
```

:::*****>> ERROR <<*****

```
(3) 005252 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.  
(3) ;/BIT 5 FAILED TO CLEAR.  
(4)
```

:::*****>> ERROR <<*****

```
(3) 005254 2$:
```



```

(3)                                     ;/#
(7) .....
(6) *TEST 32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) .....
(6) TST32: SCOPE
(5) 005354 000004                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                                         ;/SET BIT 7.
(3)                                                         ;/SET FOR ERROR TYPEOUT S/B.
(3)                                                         ;/READ THE BUFFER REGISTER.
(3) 005356 012737 000200 001124      MOV      #BIT7,$GDDAT
(4)                                     ;*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*      MOV      @ABR,$BDDAT     ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(4)                                     ;*      CMP      $GDDAT,$BDDAT  ;/DID BIT 7 AND ONLY BIT 7 SET?
(3) 005404 023737 001124 001126      BEQ      1$                    ;/IF SO-LETS TRY CLEARING IT.
(3) 005412 001402
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 005414 104003      ERROR      3                    ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                                         ;/BIT 7 FAILED TO BIT SET.
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 005416 000416      BR          2$                    ;/BR TO END SUBTEST.
(5) 005420      1$:      CLR          $GDDAT           ;/TRY CLEARING BIT 7.
(3) 005420 005037 001124      ;*      MOV      $GDDAT,@ABR      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;*      MOV      @ABR,$BDDAT     ;/NOW READ IT BACK.
(4)                                     ;*      TST      $BDDAT
(4)                                     ;*      BEQ      2$                    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005444 005737 001126
(3) 005450 001401      ;/IF ZERO-NO ERROR!
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 005452 104003      ERROR      3                    ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                                         ;/BIT 7 FAILED TO CLEAR.
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 005454      2$:

```

```
(3) ;/ #
(7) :*****
(6) :*TEST 33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 005454 000004 TST33: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 8.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 005456 012737 000400 001124 MOV #BIT8,$GDDAT
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005504 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 8 AND ONLY BIT 8 SET?
(3) 005512 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::*****>> ERROR <<*****
(3) 005514 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 8 FAILED TO BIT SET.
(4)
(4) :::*****>> ERROR <<*****
(3) 005516 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 005520 1$: ;/TRY CLEARING BIT 8.
(3) 005520 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005544 005737 001126 TST $BDDAT
(3) 005550 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(4) :::*****>> ERROR <<*****
(3) 005552 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 8 FAILED TO CLEAR.
(4)
(4) :::*****>> ERROR <<*****
(3) 005554 2$:
```



```
(3)                                     :/#
(7)                                     :*****
(6) *TEST 34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 005554 000004 TST34: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 9.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 005556 012737 001000 001124      MOV    #BIT9,$GDDAT
(4)                                     :
(4) * MOV    $GDDAT,@ABR      :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) * MOV    @ABR,$BDDAT     :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005604 023737 001124 001126      CMP    $GDDAT,$BDDAT     :/DID BIT 9 AND ONLY BIT 9 SET?
(3) 005612 001402                      BEQ    1$                :/IF SO-LETS TRY CLEARING IT.
(4)                                     :
(4) :::*****>> ERROR <<*****
(3) 005614 104003                      ERROR 3                  :/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     :/BIT 9 FAILED TO BIT SET.
(4)                                     :
(4) :::*****>> ERROR <<*****
(3) 005616 000416                      BR     2$                :/BR TO END SUBTEST.
(3) 005620 1$:                          :/TRY CLEARING BIT 9.
(3) 005620 005037 001124      CLR    $GDDAT           :/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     :/NOW READ IT BACK.
(4)                                     :
(4) * MOV    $GDDAT,@ABR     :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) * MOV    @ABR,$BDDAT     :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005644 005737 001126      TST    $BDDAT
(3) 005650 001401                      BEQ    2$                :/IF ZERO-NO ERROR!
(4)                                     :
(4) :::*****>> ERROR <<*****
(3) 005652 104003                      ERROR 3                  :/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     :/BIT 9 FAILED TO CLEAR.
(4)                                     :
(4) :::*****>> ERROR <<*****
(3) 005654                      2$:
```

```
(3)                                     :/R
(7) :*****
(6) :*TEST 35      *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 005654 000004 TST35: SCOPE
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 10.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 005656 012737 002000 001124      MOV      #BIT10,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV      @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005704 023737 001124 001126      CMP      $GDDAT,$BDDAT ;/DID BIT 10 AND ONLY BIT 10 SET?
(3) 005712 001402                      BEQ      1$             ;/IF SO-LETS TRY CLEARING IT.
(4)                                     :::*****>> ERROR <<*****
(3) 005714 104003                      ERROR    3             ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 10 FAILED TO BIT SET.
(4)                                     :::*****>> ERROR <<*****
(3) 005716 000416                      BR       2$           ;/BR TO END SUBTEST.
(3) 005720                                1$:          ;/TRY CLEARING BIT 10.
(3) 005720 005037 001124      CLR      $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     ;* MOV      $GDDAT,@ABR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV      @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 005744 005737 001126      TST      $BDDAT
(3) 005750 001401      BEQ      2$           ;/IF ZERO-NO ERROR!
(4)                                     :::*****>> ERROR <<*****
(3) 005752 104003                      ERROR    3             ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 10 FAILED TO CLEAR.
(4)                                     :::*****>> ERROR <<*****
(3) 005754                                2$:
```



```
(3)                                     :/#
(7)                                     :*****
(6) *TEST 37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) *
(5) 006054 000004 TST37: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 12.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 006056 012737 010000 001124 MOV #BIT12,$GDDAT
(4)                                     :
(4) * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) *
(4) * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006104 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 12 AND ONLY BIT 12 SET?
(3) 006112 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006114 104003 ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
(3) ;/BIT 12 FAILED TO BIT SET.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006116 000416 BR 2$ ;/BR TO END SUBTEST.
(5) 006120 1$: ;/TRY CLEARING BIT 12.
(3) 006120 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4)
(4) * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) *
(4) * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006144 005737 001126 TST $BDDAT
(3) 006150 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006152 104003 ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
(3) ;/BIT 12 FAILED TO CLEAR.
(4)
(4) :::$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006154 2$:
```

```
(3)                                     :/ #
(7) :*****
(6) :*TEST 40      *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006154 000004 . TST40: SCOPE
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 13.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 006156 012737 020000 001124      MOV    #BIT13,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV    $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV    @ABR,$BDDAT    ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006204 023737 001124 001126      CMP    $GDDAT,$BDDAT ;/DID BIT 13 AND ONLY BIT 13 SET?
(3) 006212 001402                      BEQ    1$             ;/IF SO-LETS TRY CLEARING IT.
(4)                                     ;*
(4)                                     :::*****>> ERROR <<*****
(3) 006214 104003                      ERROR  3             ;/ERROR CLOCK AS BUFFER REGISTER.
(3)                                     ;/BIT 13 FAILED TO BIT SET.
(4)                                     :::*****>> ERROR <<*****
(3) 006216 000416                      BR     2$           ;/BR TO END SUBTEST.
(3) 006220                                1$:              ;/TRY CLEARING BIT 13.
(3) 006220 005037 001124              CLR    $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     ;* MOV    $GDDAT,@ABR  ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4)                                     ;*
(4)                                     ;* MOV    @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(3) 006244 005737 001126              TST    $BDDAT
(3) 006250 001401                      BEQ    2$           ;/IF ZERO-NO ERROR!
(4)                                     :::*****>> ERROR <<*****
(3) 006252 104003                      ERROR  3             ;/ERROR-CLOCK A BUFFER REGISTER.
(3)                                     ;/BIT 13 FAILED TO CLEAR.
(4)                                     :::*****>> ERROR <<*****
(3) 006254                                2$:
```

```
(3)
(7)
(6)
(7)
(7)
(7)
(8)
(8)
(8)
(7)
(6)
(5) 006254 000004
(3)
(3)
(3)
(3)
(3) 006256 012737 040000 001124
(4)
(4)
(4)
(4)
(3) 006304 023737 001124 001126
(3) 006312 001402
(4)
  :::$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006314 104003
(3)
(4)
  :::$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006316 000416
(3) 006320
(3) 006320 005037 001124
(3)
(4)
(4)
(4)
(4)
(3) 006344 005737 001126
(3) 006350 001401
(4)
  :::$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006352 104003
(3)
(4)
  :::$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$
(3) 006354
```

```
;/#
*****
*TEST 41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
*
*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
*F/FS OR GATES
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
*
*****
TST41: SCOPE
;/CLEAR THE BUFFER REGISTER.
;/SET BIT 14.
;/SET FOR ERROR TYPEOUT S/B.
;/READ THE BUFFER REGISTER.
MOV #BIT14,$GDDAT
; * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
; * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
CMP $GDDAT,$BDDAT ;/DID BIT 14 AND ONLY BIT 14 SET?
BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.

ERROR 3 ;/ERROR CLOCK AS BUFFER REGISTER.
;/BIT 14 FAILED TO BIT SET.

1$: BR 2$ ;/BR TO END SUBTEST.
;/TRY CLEARING BIT 14.
CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
;/NOW READ IT BACK.

; * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
; * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
TST $BDDAT
BEQ 2$ ;/IF ZERO-NO ERROR!

ERROR 3 ;/ERROR-CLOCK A BUFFER REGISTER.
;/BIT 14 FAILED TO CLEAR.

2$:
```

```

(3)                                     :/#
(7) :*****
(6) :*TEST 42          *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK A BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 006354 000004  TST42: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 15.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 006356 012737 100000 001124  MOV    #BIT15,$GDDAT
(4)                                     :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV    $GDDAT,@ABR
(4)                                     :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(4) ;* MOV    @ABR,$BDDAT
(3) 006404 023737 001124 001126  CMP    $GDDAT,$BDDAT
(3) 006412 001402                BEQ    1$
(4)                                     :/DID BIT 15 AND ONLY BIT 15 SET?
(4)                                     :/IF SO-LETS TRY CLEARING IT.
(4) :::*****>> ERROR <<*****
(3) 006414 104003                ERROR 3
(3)                                     :/ERROR CLOCK AS BUFFER REGISTER.
(4)                                     :/BIT 15 FAILED TO BIT SET.
(4) :::*****>> ERROR <<*****
(3) 006416 000416                BR     2$
(3) 006420                1$:      :/BR TO END SUBTEST.
(3) 006420 005037 001124  CLR    $GDDAT
(4)                                     :/TRY CLEARING BIT 15.
(4)                                     :/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     :/NOW READ IT BACK.
(4) ;* MOV    $GDDAT,@ABR
(4)                                     :/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(4) ;* MOV    @ABR,$BDDAT
(3) 006444 005737 001126  TST    $BDDAT
(3) 006450 001401                BEQ    2$
(4)                                     :/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
(4)                                     :/IF ZERO-NO ERROR!
(4) :::*****>> ERROR <<*****
(3) 006452 104003                ERROR 3
(3)                                     :/ERROR-CLOCK A BUFFER REGISTER.
(4)                                     :/BIT 15 FAILED TO CLEAR.
(4) :::*****>> ERROR <<*****
(3) 006454                2$:
(1)
(2)

```

```
(3)                               :/#
(7)                               :*****
(6) *TEST 43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6)                               :*****
(5) 006454 000004 TST43: SCOPE
(3)                               :/CLEAR THE STATUS REGISTER.
(3)                               :/SET BIT 11.
(3)                               :/SET FOR ERROR TYPEOUT S/B.
(3)                               :/READ THE STATUS REGISTER.
(3) 006456 012737 004000 001124 MOV #BIT11,$GDDAT
(4)                               :
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)                               :
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 006504 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 11 AND ONLY BIT 11 SET?
(3) 006512 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)                               :
(4) :::*****>> ERROR <<*****
(3) 006514 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3)                               :/BIT 11 FAILED TO BIT SET.
(4)                               :
(4) :::*****>> ERROR <<*****
(3) 006516 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 006520 1$: ;/TRY CLEARING BIT 11.
(3) 006520 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                               :/NOW READ IT BACK.
(4)                               :
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)                               :
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 006544 005737 001126 TST $BDDAT
(3) 006550 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)                               :
(4) :::*****>> ERROR <<*****
(3) 006552 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3)                               :/BIT 11 FAILED TO CLEAR.
(4)                               :
(4) :::*****>> ERROR <<*****
(3) 006554 2$:
(2)
```



```
(3)                                     :/ #
(7) :*****
(6) *TEST 45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' ? OCCURANCES PER PAS.
(8) *
(7) :*****
(6) TST45: SCOPE
(5) 006654 000004                                     :/CLEAR THE STATUS REGISTER.
(3)                                                     :/SET BIT 6.
(3)                                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                                     :/READ THE STATUS REGISTER.
(3) 006656 012737 000100 001124      MOV      #BIT6,$GDDAT
(4)
(4)      ;*      MOV      $GDDAT,@BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)      ;*      MOV      @BSR,$BDDAT     ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 006704 023737 001124 001126      CMP      $GDDAT,$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?
(3) 006712 001402                      BEQ      1$           ;/IF SO-LETS TRY CLEARING IT.
(4)
(4)      :::*****>> ERROR <<*****
(3) 006714 104005                      ERROR 5           ;/ERROR CLOCK BS STATUS REGISTER.
(3)                                     ;/BIT 6 FAILED TO BIT SET.
(4)
(4)      :::*****>> ERROR <<*****
(3) 006716 000416                      BR      2$           ;/BR TO END SUBTEST.
(3) 006720 1$:                          ;/TRY CLEARING BIT 6.
(3) 006720 005037 001124      CLR      $GDDAT     ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                                     ;/NOW READ IT BACK.
(4)
(4)      ;*      MOV      $GDDAT,@BSR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)      ;*      MOV      @BSR,$BDDAT     ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 006744 005737 001126      TST      $BDDAT
(3) 006750 001401                      BEQ      2$           ;/IF ZERO-NO ERROR!
(4)
(4)      :::*****>> ERROR <<*****
(3) 006752 104005                      ERROR 5           ;/ERROR-CLOCK B STATUS REGISTER.
(3)                                     ;/BIT 6 FAILED TO CLEAR.
(4)
(4)      :::*****>> ERROR <<*****
(3) 006754      2$:
(2)
```

```
(3)                               ;/#
(7)                               :*****
(6) *TEST 46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6)                               :*****
(5) 006754 000004 TST46: SCOPE
(3)                               ;/CLEAR THE STATUS REGISTER.
(3)                               ;/SET BIT 5.
(3)                               ;/SET FOR ERROR TYPEOUT S/B.
(3)                               ;/READ THE STATUS REGISTER.
(3) 006756 012737 000040 001124      MOV    #BITS,$GDDAT
(4)                               ;*
(4)                               ;* MOV    $GDDAT,@BSR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)                               ;*
(4)                               ;* MOV    @BSR,$BDDAT  ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007004 023737 001124 001126      CMP    $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(3) 007012 001402                      BEQ    1$           ;/IF SO-LETS TRY CLEARING IT.
(4)
      :::*****>> ERROR <<*****
(3) 007014 104005                      ERROR 5           ;/ERROR CLOCK BS STATUS REGISTER.
(3)                               ;/BIT 5 FAILED TO BIT SET.
(4)
      :::*****>> ERROR <<*****
(3) 007016 000416                      BR     2$           ;/BR TO END SUBTEST.
(5) 007020 1$:                          ;/TRY CLEARING BIT 5.
(3) 007020 005037 001124      CLR    $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3)                               ;/NOW READ IT BACK.
(4)
(4)                               ;*
(4)                               ;* MOV    $GDDAT,@BSR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4)                               ;*
(4)                               ;* MOV    @BSR,$BDDAT  ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007044 005737 001126      TST    $BDDAT
(3) 007050 001401                      BEQ    2$           ;/IF ZERO-NO ERROR!
(4)
      :::*****>> ERROR <<*****
(3) 007052 104005                      ERROR 5           ;/ERROR-CLOCK B STATUS REGISTER.
(3)                               ;/BIT 5 FAILED TO CLEAR.
(4)
      :::*****>> ERROR <<*****
(3) 007054 2$:
(2)
```



```
(3) ;/#
(7) :*****
(6) :*TEST 50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 007154 000004 TST50: SCOPE ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 3.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 007156 012737 000010 001124 MOV #BIT3,$GDDAT
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(4) CMP $GDDAT,$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(3) 007204 023737 001124 001126 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3) 007212 001402
(4) :::*****>> ERROR <<*****
(3) 007214 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 3 FAILED TO BIT SET.
(4) :::*****>> ERROR <<*****
(3) 007216 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 007220 1$: ;/TRY CLEARING BIT 3.
(3) 007220 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007244 005737 001126 TST $BDDAT
(3) 007250 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4) :::*****>> ERROR <<*****
(3) 007252 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 3 FAILED TO CLEAR.
(4) :::*****>> ERROR <<*****
(3) 007254 2$:
(2)
```

```
(3) ;/M
(7) :*****
(6) *TEST 51 *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) *
(6) :*****
(5) 007254 000004 TST51: SCOPE
(3) ;/CLEAR THE STATUS REGISTER.
(3) ;/SET BIT 2.
(3) ;/SET FOR ERROR TIMEOUT S/B.
(3) ;/READ THE STATUS REGISTER.
(3) 007256 012737 000004 001124 MOV #BIT2,$GDDAT
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(4) ;* CMP $GDDAT,$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(3) 007304 023737 001124 001126 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(3) 007312 001402
(4) :::*****>> ERROR <<*****
(3) 007314 104005 ERROR 5 ;/ERROR CLOCK BS STATUS REGISTER.
(3) ;/BIT 2 FAILED TO BIT SET.
(4) :::*****>> ERROR <<*****
(3) 007316 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 007320 1$: ;/TRY CLEARING BIT 2.
(3) 007320 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(3) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(4) ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
(3) 007344 005737 001126 TST $BDDAT
(3) 007350 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4) :::*****>> ERROR <<*****
(3) 007352 104005 ERROR 5 ;/ERROR-CLOCK B STATUS REGISTER.
(3) ;/BIT 2 FAILED TO CLEAR.
(4) :::*****>> ERROR <<*****
(3) 007354 2$:
(2)
```



```

(3)                               :/#
(7)                               :*****
(6) *TEST 54 *TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
(7)                               :*
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8)                               :*
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8)                               :*
(7)                               :*
(6)                               :*****
(5) 007554 000004 TST54: SCOPE
(3)                               :/CLEAR THE BUFFER REGISTER.
(3)                               :/SET BIT 0.
(3)                               :/SET FOR ERROR TYPEOUT S/B.
(3)                               :/READ THE BUFFER REGISTER.
(3) 007556 012737 000001 001124 MOV #BIT0,$GDDAT
(4)                               :/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV $GDDAT,@BBR
(4)                               :/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(4) ;* MOV @BBR,$BDDAT
(3) 007604 023737 001124 001126 CMP $GDDAT,$BDDAT
(3) 007612 001402 BEQ 1$
(4)                               :/IF SO-LETS TRY CLEARING IT.
:::*****>> ERROR <<*****
(3) 007614 104006 ERROR 6
(3)                               :/ERROR CLOCK BS BUFFER REGISTER.
(4)                               :/BIT 0 FAILED TO BIT SET.
:::*****>> ERROR <<*****
(3) 007616 000416 BR 2$
(3) 007620 1$:
(3) 007620 005037 001124 CLR $GDDAT
(4)                               :/BR TO END SUBTEST.
(4)                               :/TRY CLEARING BIT 0.
(4)                               :/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                               :/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BBR
(4)                               :/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,$BDDAT
(3) 007644 005737 001126 TST $BDDAT
(3) 007650 001401 BEQ 2$
(4)                               :/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(4)                               :/IF ZERO-NO ERROR!
:::*****>> ERROR <<*****
(3) 007652 104006 ERROR 6
(3)                               :/ERROR-CLOCK B BUFFER REGISTER.
(4)                               :/BIT 0 FAILED TO CLEAR.
:::*****>> ERROR <<*****
(3) 007654 2$:

```

```
(3)                                     ;/N
(7) :*****
(6) *TEST 55 *TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
(7) *
(7) *CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) *F/FS OR GATES
(8) *
(8) * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) *
(7) :*****
(6) :*****
(5) 007654 000004 TST55: SCOPE
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 1.
(3)                                     ;/SET FOR ERROR TIMEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 007656 012737 000002 001124 MOV #BIT1,$GDDAT
(4)                                     ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) * MOV $GDDAT,@BBR ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(4) * MOV @BBR,$BDDAT ;/DID BIT 1 AND ONLY BIT 1 SET?
(3) 007704 023737 001124 001126 CMP $GDDAT,$BDDAT ;/IF SO-LETS TRY CLEARING IT.
(3) 007712 001402 BEQ 1$
(4)
(4) :::*****>> ERROR <<*****
(3) 007714 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 1 FAILED TO BIT SET.
(4)
(4) :::*****>> ERROR <<*****
(3) 007716 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 007720 1$: ;/TRY CLEARING BIT 1.
(3) 007720 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4) ;/NOW READ IT BACK.
(4) * MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) * MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 007744 005737 001126 TST $BDDAT
(3) 007750 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(4) :::*****>> ERROR <<*****
(3) 007752 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 1 FAILED TO CLEAR.
(4)
(4) :::*****>> ERROR <<*****
(3) 007754 2$:
```



```
(3)                                     :/N
(7) :*****
(6) :*TEST 57 *TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010054 000004 TST57: SCOPE
(3)                                     :/CLEAR THE BUFFER REGISTER.
(3)                                     :/SET BIT 3.
(3)                                     :/SET FOR ERROR TYPEOUT S/B.
(3)                                     :/READ THE BUFFER REGISTER.
(3) 010056 012737 000010 001124 MOV #BIT3,$GDDAT
(4)                                     :/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) :* MOV $GDDAT,@BBR
(4)                                     :/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(4) :* MOV @BBR,$BDDAT
(3) 010104 023737 001124 001126 CMP $GDDAT,$BDDAT
(3) 010112 001402 BEQ 1$
(4)                                     :/DID BIT 3 AND ONLY BIT 3 SET?
(4)                                     :/IF SO-LETS TRY CLEARING IT.
(4) :::*****>> ERROR <<*****
(3) 010114 104006 ERROR 6
(3)                                     :/ERROR CLOCK BS BUFFER REGISTER.
(4)                                     :/BIT 3 FAILED TO BIT SET.
(4) :::*****>> ERROR <<*****
(3) 010116 000416 BR 2$
(3) 010120 1$:
(3) 010120 005037 001124 CLR $GDDAT
(4)                                     :/BR TO END SUBTEST.
(4)                                     :/TRY CLEARING BIT 3.
(4)                                     :/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     :/NOW READ IT BACK.
(4) :* MOV $GDDAT,@BBR
(4)                                     :/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) :* MOV @BBR,$BDDAT
(3) 010144 005737 001126 TST $BDDAT
(3) 010150 001401 BEQ 2$
(4)                                     :/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(4)                                     :/IF ZERO-NO ERROR!
(4) :::*****>> ERROR <<*****
(3) 010152 104006 ERROR 6
(3)                                     :/ERROR-CLOCK B BUFFER REGISTER.
(4)                                     :/BIT 3 FAILED TO CLEAR.
(4) :::*****>> ERROR <<*****
(3) 010154 2$:
```

```
(3)                                     :/#
(7) :*****
(6) :*TEST 60      *TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010154 000004 TST60: SCOPE
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 4.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 010156 012737 000020 001124      MOV    #BIT4,$GDDAT
(4)                                     ;*
(4)                                     MOV    $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     MOV    @BBR,$BDDAT    ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010204 023737 001124 001126      CMP    $GDDAT,$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?
(3) 010212 001402                      BEQ    1$           ;/IF SO-LETS TRY CLEARING IT.
(4)                                     :::*****>> ERROR <<*****
(3) 010214 104006                      ERROR  6           ;/ERROR CLOCK BS BUFFER REGISTER.
(3)                                     ;/BIT 4 FAILED TO BIT SET.
(4)                                     :::*****>> ERROR <<*****
(3) 010216 000416                      BR     2$         ;/BR TO END SUBTEST.
(3) 010220 1$:                          CLR    $GDDAT    ;/TRY CLEARING BIT 4.
(3) 010220 005037 001124                ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     MOV    $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     MOV    @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010244 005737 001126                TST    $BDDAT
(3) 010250 001401                      BEQ    2$         ;/IF ZERO-NO ERROR!
(4)                                     :::*****>> ERROR <<*****
(3) 010252 104006                      ERROR  6           ;/ERROR-CLOCK B BUFFER REGISTER.
(3)                                     ;/BIT 4 FAILED TO CLEAR.
(4)                                     :::*****>> ERROR <<*****
(3) 010254 2$:
```

```
(3)                                     ;/#
(7) :*****
(6) :*TEST 61      *TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010254 000004 TST61: SCOPE
(3)                                     ;/CLEAR THE BUFFER REGISTER.
(3)                                     ;/SET BIT 5.
(3)                                     ;/SET FOR ERROR TYPEOUT S/B.
(3)                                     ;/READ THE BUFFER REGISTER.
(3) 010256 012737 000040 001124      MOV    #BIT5,$GDDAT
(4)                                     ;*
(4)                                     ;* MOV    $GDDAT,@BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     ;* MOV    @BBR,$BDDAT    ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010304 023737 001124 001126      CMP    $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(3) 010312 001402                      BEQ    1$             ;/IF SO-LETS TRY CLEARING IT.
(4)
(4)      ;:::*****>> ERROR <<*****
(3) 010314 104006                      ERROR  6             ;/ERROR CLOCK BS BUFFER REGISTER.
(3)                                     ;/BIT 5 FAILED TO BIT SET.
(4)
(4)      ;:::*****>> ERROR <<*****
(3) 010316 000416                      BR     2$           ;/BR TO END SUBTEST.
(3) 010320                      1$:                ;/TRY CLEARING BIT 5.
(3) 010320 005037 001124      CLR    $GDDAT      ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4)                                     ;/NOW READ IT BACK.
(4)                                     ;*
(4)                                     ;* MOV    $GDDAT,@BBR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4)                                     ;*
(4)                                     ;* MOV    @BBR,$BDDAT    ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010344 005737 001126      TST    $BDDAT
(3) 010350 001401                      BEQ    2$           ;/IF ZERO-NO ERROR!
(4)
(4)      ;:::*****>> ERROR <<*****
(3) 010352 104006                      ERROR  6             ;/ERROR-CLOCK B BUFFER REGISTER.
(3)                                     ;/BIT 5 FAILED TO CLEAR.
(4)
(4)      ;:::*****>> ERROR <<*****
(3) 010354                      2$:
```

```
(3) ;/#
(7) :*****
(6) :*TEST 62 *TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
(7) :*
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(7) :*F/FS OR GATES
(8) :*
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(8) :*
(7) :*
(6) :*****
(5) 010354 000004 TST62: SCOPE
(3) ;/CLEAR THE BUFFER REGISTER.
(3) ;/SET BIT 6.
(3) ;/SET FOR ERROR TYPEOUT S/B.
(3) ;/READ THE BUFFER REGISTER.
(3) 010356 012737 000100 001124 MOV #BIT6,$GDDAT
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010404 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?
(3) 010412 0C1402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(4)
(4) :::*****>> ERROR <<*****
(3) 010414 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.
(3) ;/BIT 6 FAILED TO BIT SET.
(4)
(4) :::*****>> ERROR <<*****
(3) 010416 000416 BR 2$ ;/BR TO END SUBTEST.
(3) 010420 1$: ;/TRY CLEARING BIT 6.
(3) 010420 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(4) ;/NOW READ IT BACK.
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
(3) 010444 005737 001126 TST $BDDAT
(3) 010450 001401 BEQ 2$ ;/IF ZERO-NO ERROR!
(4)
(4) :::*****>> ERROR <<*****
(3) 010452 104006 ERROR 6 ;/ERROR-CLOCK B BUFFER REGISTER.
(3) ;/BIT 6 FAILED TO CLEAR.
(4)
(4) :::*****>> ERROR <<*****
(3) 010454 2$:
```

```
(3) ;/H  
(7) :*****  
(6) :*TEST 63 *TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED  
(7) :*  
(7) :*CLOCK B BUFFER REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
(7) :*F/FS OR GATES  
(8) :*  
(8) :* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS  
(8) :*  
(7) :*  
(6) :*****  
(5) 010454 000004 TST63: SCOPE  
(3) ;/CLEAR THE BUFFER REGISTER.  
(3) ;/SET BIT 7.  
(3) ;/SET FOR ERROR TYPEOUT S/B.  
(3) ;/READ THE BUFFER REGISTER.  
(3) 010456 012737 000200 001124 MOV #BIT7,$GDDAT  
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.  
(3) 010504 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 7 AND ONLY BIT 7 SET?  
(3) 010512 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.  
(4) :::*  
(3) 010514 104006 ERROR 6 ;/ERROR CLOCK BS BUFFER REGISTER.  
(3) ;/BIT 7 FAILED TO BIT SET.  
(4) :::*  
(3) 010516 000416 BR 2$ ;/BR TO END SUBTEST.  
(3) 010520 1$: ;/TRY CLEARING BIT 7.  
(3) 010520 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.  
(3) ;/NOW READ IT BACK.  
(4) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
(4) ;* MOV @BBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.  
(3) 010544 005737 001126 TST $BDDAT  
(3) 010550 001401 BEQ 2$ ;/IF ZERO-NO ERROR!  
(4) :::*  
(3) 010552 104006 ERROR 6 ;/ERROR-CLOCK B BUFFEP REGISTER.  
(3) ;/BIT 7 FAILED TO CLEAR.  
(4) :::*  
(3) 010554 2$:  
1779 .SBTTL *  
1780 .SBTTL * PHASE 2 ADVANCED BASIC LOGIC TESTS  
1781 .SBTTL *  
1782  
1788  
1789 :*****
```



```
(3) ;*TEST 64 *TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
(4)
(5)
(5) ;*
(5) ;*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) ;*F/FS OR GATES
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(6) ;*
(5) ;*
(4)
(3) ;*****
(2) 010554 000004 TST64: SCOPE
1790
1791 ;SELECT MODE 0.
1792 ;CLEAR THE BUFFER REGISTER. BUFFER
1793 ;REGISTER WILL BE TRANSFERRED TO
1794 ;COUNT REGISTER SINCE THIS IS MODE 0.
1795 010556 005037 001124 CLR $GDDAT
1796
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
1797 ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1)
1798
1799 010602 005037 001124 CLR $GDDAT ;EXPECT TO READ BACK ALL 0'S.
1800 ;READ THE COUNT REGISTER - IT SHOULD BE CLEAR.
1801
(1) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
1802 010616 005737 001126 TST $BDDAT
1803 010622 001401 BEQ 1$ ;BR IF YES TO NEXT TEST
1804
1805
:::*****>> ERROR <<*****
1806 010624 104004 ERROR 4 ;ERROR - CLOCK A'S COUNTER REGISTER
1807 ;NOT CLEAR.
1808
1809
:::*****>> ERROR <<*****
1810 010626 1$:
1811
1812 ;*****
(3) ;*TEST 65 *TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
(4)
(5) ;*
(5) ;*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) ;*F/FS OR GATES
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(6) ;*
(5) ;*
(4)
(3) ;*****
(2) 010626 000004 TST65: SCOPE
1813
1814 ;SELECT MODE 0.
```

```

1815 ;LOAD THE BUFFER REGISTER WITH
1816 ;PATTERN 125252. IT WILL BE
1817 ;TRANSFERRED TO THE COUNT REGISTER
1818 ;SINCE THIS IS MODE 0.
1819 010630 005037 001124 CLR $GDDAT
1820 (1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
1821 010644 012737 125252 001124 MOV #125252,$GDDAT ;SET EXPECTED TO PATTERN IN CASE OF
1822 ;NEED OF ERROR TYPEOUT.
1823 ;READ THE COUNT REGISTER
1824 (1) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
1825 (1) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
1826 010672 023737 001124 001126 CMP $GDDAT,$BDDAT ;DID ALL THE BITS AND NO OTHER BITS
1827 ;COME THROUGH?
1828 010700 001401 BEQ 1$ ;BR IF YES TO NEXT TEST.
1829
1830
1831
1832

```

::: \$ ERROR << \$

```

1833 010702 104004 ERROR 4 ;DATA ERROR CLOCK A PATTERN '125252'
1834 ;FAILED TO TRANSFER PROPERLY BETWEEN
1835 ;BUFFER AND COUNT REGISTERS.
1836
1837

```

::: \$ ERROR << \$

```

1838 010704 1$:
1839
1840 ;*****
1841 (3) ;*TEST 66 *TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
1842 (4)
1843 (5) ;*
1844 (5) ;*CLOCK A COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
1845 (5) ;*F/FS OR GATES
1846 (6) ;*
1847 (6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
1848 (6) ;*
1849 (5) ;*
1850 (4)
1851 (3) ;*****

```

TST66: SCOPE

```

1841 (2) 010704 000004 ;SELECT MODE 0.
1842
1843 010706 005037 001124 CLR $GDDAT
1844 (1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
1845 ;LOAD THE BUFFER REGISTER WITH
1846 ;PATTERN 052525. IT WILL BE
1847 ;TRANSFERRED TO THE COUNT REGISTER
1848 ;SINCE THIS IS MODE 0.
1849
1850 010722 012737 052525 001124 MOV #052525,$GDDAT ;SET EXPECTED TO PATTERN IN CASE OF

```

```
1851                                     ;NEED OF ERROR TIMEOUT.  
1852                                     ;READ THE COUNT REGISTER  
1853  
1854                                     ;* MCV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
1855                                     ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
1856 010750 023737 001124 001126          CMP $GDDAT,$BDDAT ;DID ALL THE BITS AND NO OTHER BITS  
1857                                     ;COME THROUGH?  
1858 010756 001401                          BEQ 1$            ;BR IF YES TO NEXT TEST.  
1859  
1860  
      ;:;$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
1861 010760 104004                          ERROR 4           ;DATA ERROR CLOCK A PATTERN '052525'  
1862                                     ;FAILED TO TRANSFER PROPERLY BETWEEN  
1863                                     ;BUFFER AND COUNT REGISTERS.  
1864  
1865  
      ;:;$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
1866 010762                                1$:  
1867  
1873  
1874 ;:;*****  
1875 (3) ;*TEST 67 *TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR  
1876 (4)  
1877 (5) ;*  
1878 (5) ;*CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL  
1879 (5) ;*F/FS OR GATES  
1880 (6) -----  
1881 (6) ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS  
1882 (6) ;*  
1883 (5) ;*  
1884 (4) ;:;*****  
1885 (3) ;*  
1886 (2) 010762 000004 TST67: SCOPE  
1887                                     ;SELECT MODE 0.  
1888                                     ;CLEAR THE BUFFER REGISTER. BUFFER  
1889                                     ;REGISTER WILL BE TRANSFERRED TO  
1890                                     ;COUNT REGISTER SINCE THIS IS MODE 0.  
1880 010764 005037 001124          CLR $GDDAT  
1881 (1) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
1882 (1) ;* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
1883 011010 005037 001124          CLR $GDDAT  
1884                                     ;EXPECT TO READ BACK ALL 0'S.  
1885                                     ;READ THE COUNT REGISTER - IT SHOULD BE CLEAR.  
1886 (1) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
1887 011024 005737 001126          TST $BDDAT  
1888 011030 001401                          BEQ 1$            ;BR IF YES TO NEXT TEST  
1889  
1890
```

```

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS
1891 011032 104007            ERROR 7             ;ERROR - CLOCK B'S COUNTER REGISTER
1892                                     ;NOT CLEAR.
1893
1894

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS

1895 011034                1$:
1896
1897
1898          :*****
(3)          ;*TEST 70      *TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN
(4)
(5)
(5)          ;*CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5)          ;*F/FS OR GATES
(6)
(6)          ;* PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
(6)          ;*
(5)          ;*
(4)
(3)          :*****
(2) 011034 000004          TST70: SCOPE
1899
1900                                     ;SELECT MODE 0.
1901 011036 005037 001124          CLR      $GDDAT
1902          ;*      MOV      $GDDAT,@BSR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(1)          ;LOAD THE BUFFER REGISTER WITH
1903          ;PATTERN 125. IT WILL BE
1904          ;TRANSFERRED TO THE COUNT REGISTER
1905          ;SINCE THIS IS MODE 0.
1906
1907 011052 012737 000125 001124          MOV      #125,$GDDAT          ;SET EXPECTED TO PATTERN IN CASE OF
1908          ;*      MOV      $GDDAT,@BBR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
1909          ;NEED OF ERROR TIMEOUT.
1910          ;READ THE COUNT REGISTER
1911
1912          ;*      MOV      @BCR,$BDDAT          ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1)
1913
1914 011100 023737 001124 001126          CMP      $GDDAT,$BDDAT          ;DID ALL THE BITS AND NO OTHER BITS
1915          ;COME THROUGH?
1916 011106 001401          BEQ      1$          ;BR IF YES TO NEXT TEST.
1917
1918

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS

1919 011110 104007            ERROR 7             ;DATA ERROR CLOCK B - PATTERN '125'
1920                                     ;FAILED TO TRANSFER PROPERLY BETWEEN
1921                                     ;BUFFER AND COUNT REGISTERS.
1922
1923

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS

```

1924 011112

1925
1926

(3)
(4)
(5)
(5)
(5)
(6)
(6)
(6)
(5)
(4)
(3)

1\$:

: *TEST 71 *TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
:
: *CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
: *F/FS OR GATES
:
: * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 OCCURANCES PER PASS
:
: *

(2) 011112 000004

TST71: SCOPE

1927

: SELECT MODE 0.

1928

1929 011114 005037 001124

CLR \$GDDAT

1930

: * MOV \$GDDAT,@BSR ; / PUT DATA FROM \$GDDAT TO DEVICE REG BSR
: * ; LOAD THE BUFFER REGISTER WITH
: * ; PATTERN 252. IT WILL BE
: * ; TRANSFERRED TO THE COUNT REGISTER
: * ; SINCE THIS IS MODE 0.

(1)

1931

1932

1933

1934

1935

1936 011130 012737 000252 001124

MOV #252,\$GDDAT ; SET EXPECTED TO PATTERN IN CASE OF

1937

(1)

: * MOV \$GDDAT,@BBR ; / PUT DATA FROM \$GDDAT TO DEVICE REG BBR
: * ; NEED OF ERROR TYPEOUT.
: * ; READ THE COUNT REGISTER

1938

1939

1940

(1)

: * MOV @BCR,\$BDDAT ; / READ DEVICE REG BCR, PUT DATA IN \$BDDAT.

1941

1942 011156 023737 001124 001126

CMP \$GDDAT,\$BDDAT ; DID ALL THE BITS AND NO OTHER BITS

1943

1944 011164 001401

BEQ 1\$; COME THROUGH?
; BR IF YES TO NEXT TEST.

1945

1946

::: \$ >> ERROR << \$

1947 011166 104007

ERROR 7 ; DATA ERROR CLOCK B - PATTERN '252'

1948

1949

1950

1951

; FAILED TO TRANSFER PROPERLY BETWEEN
; BUFFER AND COUNT REGISTERS.

::: \$ >> ERROR << \$

1952 011170

1\$:

1953

1967

1968

(3)

: *TEST 72 *TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
:
: *

(4)

(4)

(5)

(5)

: *NEW SIGNALS GENERATION OF 'STP1' BY 'LD STAT A' H + 'BD 12' H
:
: *

: * PROBABLE SYNC POINT FOR THIS TEST:: 'DEVICE OUT' 2 PER PASS


```
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2008
(1) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
2009 011332 032737 000001 001126 ;* BIT #BIT00,$BDDAT
2010 011340 001001 ;* BNE 1$ ;BR IF YES - NEXT TEST.
2011
2012
```

:::\$>> ERROR <<\$

```
2013 011342 104001 ERROR 1 ;ERROR - BIT00 OF CLOCK A'S STATUS REGISTER
2014 ;FAILED TO SET WHEN BIT13 WAS SET
2015 ;AND A MAINTENANCE ST1 GENERATED.
2016
2017
```

:::\$>> ERROR <<\$

```
2018 011344 ;$: CLR $GDDAT ;LEAVE SUBTEST WITH CLOCK CLEAR.
2019 011344 005037 001124
2020
```

```
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2021
2023
2024
```

```
(3) ;*TEST 74 *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
(4) ;*
(4) ;*COUNT TEST - THIS IS THE VERY FIRST TIME THAT THE COUNTER
(4) ;*HAS BEEN ASKED TO INCREMENT! WHAT WE ARE GOING TO DO IS
(4) ;*CLEAR THE BUFFER, SELECT MODE 0, RATE OF STP1.
(4) ;*NEXT WILL GENERATE THE STP1 THROUGH MAINTENANCE MODE (WE'VE
(4) ;*DONE THIS BEFORE IN A PREVIOUS TEST TO SEE IF THE FLAG WOULD SET)
(4) ;*AND SEE IF THE COUNTER HAS INCREMENTED.
```

* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'

```
(3) ;*
(2) 011360 000004 TST74: SCOPE
```

```
2035 ;*
2036 ;* ;CLEAR CLOCK A.
2037 ;* ;CLEAR BUFFER REGISTER.
2038 011362 005037 001124 CLR $GDDAT
2039
```

```
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2040 ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
(1) ;* ;SELECT: MODE0! RATE 'STP1' AND ENABLE
2041 ;* ;CLOCK A TO COUNT.
2042 ;* ;NOW GENERATE A MAINTENANCE STP1 - AT
2043 ;* ;THIS TIME THE CLOCK SHOULD COUNT ONCE.
2044
```

```
2045 011406 012737 000015 001124 MOV #15,$GDDAT
2046 (1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
```

```
2047 (1) ;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
2048 011434 052737 010000 001124 ;* BIS #BIT12,$GDDAT
2049
```



```
2095                                     ;'LOOP ON TEST' (SW14=1) FEATURE. NOWMAL  
2096                                     ;LOOP BACK POINT WILL BE '2$'.  
2097  
2098 011534 012737 000015 001354      MOV    #15,$TMDAT  
2099  
2100                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
2101                                     ;ENABLE COUNTER TO COUNT. SELECTED:  
2102 011552      2$:                                     ;MODE 0, RATE "STP1"  
2103 011562 052737 010000 001354      ;*     MOV    @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
2104                                     BIS    #BIT12,$TMDAT      ;GENERATE A MAINTENANCE "STP1". THIS  
2105                                     ;*     MOV    $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
2106 011600 005237 001124      INC    $GDDAT      ;ONE VALUE.  
2107                                     ;$GDDAT IS USED TO KEEP TRACK OF THE  
2108                                     ;VALUE THE CLOCK SHOULD COUNT TO.  
2109  
2110                                     ;*     MOV    @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
2111 011614 023737 001126 001124      CMP    $BDDAT,$GDDAT      ;DID COUNT OCCUR CORRECTLY?  
2112 011622 001402      BEQ    3$          ;IF YES - BR TO "3$".  
2113  
2114
```

::: \$>> ERROR << \$

```
2115 011624 104011      ERROR    11      ;ERROR - CLOCK A FAILED TO UPCOUNT  
2116                                     ;CORRECTLY USING MODE 0 - RATE "STP1".  
2117  
2118
```

::: \$>> ERROR << \$

```
2119 011626 000403      BR      4$  
2120 011630 005737 001124      3$:     TST    $GDDAT      ;DID WE ACHIEVE OVERFLOW TO ZERO YET?  
2121 011634 001410      BEQ    5$          ;IF YES - BR NEXT TEST  
2122  
2123 011636 032777 040000 167274      4$:     BIT    #BIT14,@SWR      ;LOOP CURRENT COUNT?  
2124 011644 001742      BEQ    2$          ;BR IF NO TO NEXT COUNT UPDATE.  
2125 011646 162737 000001 001124      SUB    #1,$GDDAT      ;IF YES - DECREMENT EXPECTED AND RELOAD.  
2126 011654 000715      BR      1$          ;GOTO RELOAD POINT.  
2127  
2128 011656      5$:                                     ;END SUBTEST  
2129  
2130 .SBTTL *  
2131 .SBTTL * PHASE 3 CLOCK A COUNT FUNCTION TESTS  
2132 .SBTTL *  
2133  
2143
```

::: *****
*TEST 76 *TEST THAT CLOCK A OVERFLOW WILL OCCUR
*
*NOW WE'LL TRY AND GENERATE "A OVERFLOW L"
*WHICH SETS BD05. WE'LL DO IT BY PRESETTING THE BUFFER
*AT 177777 AND GENERATE A MAINTENANCE STP1. WE ALREADY
*KNOW MAINTENANCE STP1'S WILL ADVANCE THE COUNTER.

(3)
(4)
(4)
(4)
(4)
(4)

```
(4) ;*ALSO SEE IF 'MODE' FLG GETS SET.
(5) ;*
(5) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(5) ;*
(3) ;*****
(2) 011656 000004 TST76: SCOPE
2145 ;MAKE SURE CLOCK A CLEAR.
2146 ;
2147 011660 005037 001124 CLR $GDDAT
2148 ;
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2149 011674 012737 177777 001124 ;* MOV #177777,$GDDAT ;PRESET BUFFER TO ALL ONES.
2150 ;
(1) ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
2151 ;SELECT MODE 0; RATE STP4; GO.
2152 ;GENERATE A MAINTENANCE STP1.
2153 011712 012737 000015 001124 MOV #15,$GDDAT
2154 ;
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2155 ;
(1) ;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
2156 011740 052737 010000 001124 ;* BIS #BIT12,$GDDAT
2157 ;
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2158 ;
2159 011756 1$: ;DID OVERFLOW BIT SET?
2160 ;
(1) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
2161 011766 032737 000040 001126 ;* BIT #BIT05,$BDDAT
2162 011774 001002 BNE 2$ ;BR IF YES TO '2$'.
2163 ;
:::*****>> ERROR <<*****
2164 011776 104012 ERROR 12 ;ERROR BIT05 OF CSR CLOCK A FAILED
2165 ;TO SET ON OVERFLOW.
2166 ;
:::*****>> ERROR <<*****
2167 012000 000411 BR 3$
2168 ;
2169 012002 2$: ;DID BIT07 - 'MODE' FLG SET?
2170 ;
(1) ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
2171 012012 032737 000200 001126 ;* BIT #BIT07,$BDDAT
2172 ;IT SHOULD SET WHEN BIT05 SETS.
2173 012020 001001 BNE 3$ ;BR IF YES TO 3$.
2174 ;
:::*****>> ERROR <<*****
2175 012022 104012 ERROR 12 ;OVERFLOW FAILED TO SET CLOCK A'S
2176 ;CSR BIT07 'MODE' FLG. IT
2177 ;HAD; HOWEVER SET BIT05 'OVERFLOW'
2178 ;FLAG.
2179 ;
:::*****>> ERROR <<*****
```



```
2221                                     ;THE OVERFLOW OCCURRED?  
2222 012166 001401                      BEQ    2$    ;BR IF YES - NEXT TEST.  
2223                                     ;  
      ;:;SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS  
2224 012170 104012                      ERROR  12    ;ERROR CLOCK A - COUNTER DID NOT GET RELOAD FROM  
2225                                     ;BUFFER AFTER OVERFLOW. 'A RELOAD' H  
2226                                     ;DID GET GENERATED ON WE WOULD  
2227                                     ;HAVE GOT PREVIOUS ERROR; THEREFORE PROBLEM  
2228                                     ;MUST EXIST WITH COMBINING 'A RELOAD' H  
2229                                     ;WITH 'MODE A1 (0)' H TO GENERATE A  
2230                                     ;COUNTER LOAD.  
2231                                     ;  
      ;:;SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSS  
2232 012172                               2$:  
2280
```

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```
;/#  
*****  
*TEST 100 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1  
*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT  
*IN RATE: 1MHZ PART 1  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
*****  
TST100: SCOPE  
;/MAKE SURE CLOCK IS CLEAR.  
;/CLEAR THE BUFFER.  
;/SELECT: MODE 0, RATE 1MHZ ; GO.  
CLR $GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
MOV #1:2,$GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY  
1$: INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20  
BNE 1$ ;/DID COUNTER INCREMENT AT ALL?  
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/IF YES - BR NEXT TEST.  
;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.  
;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
BIT #BIT05,$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'  
;/F/F HAD SET.  
BNE 2$ ;/BR IF YES NEXT TEST.  
:::*****>> ERROR <<*****  
ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO  
;/COUNT RATE: 1MHZ.  
:::*****>> ERROR <<*****  
2$:
```

2282
 (1)
 (5)
 (4)
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 (6)
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 (5)
 (4)
 (3) 012304 000004
 (1)
 (1)
 (1)
 (1)
 (1) 012306 005037 001124
 (2)
 (2)
 (2)
 (1) 012332 012737 000005 001124
 (2)
 (2)
 (1) 012350 005000
 (1) 012352 005200
 (1) 012354 001376
 (1)
 (2)
 (2)
 (1) 012366 005737 001126
 (1) 012372 001011
 (1)
 (1)
 (2)
 (1) 012404 032737 000040 001126
 (1)
 (1)
 (1) 012412 001001
 (2)
 (1) 012414 104012
 (1)
 (2)
 (1) 012416

```

  :/#
  :*****
  *TEST 101 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
  *
  *THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
  *IN RATE: 100KHZ PART 1
  *
  * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
  *
  :*****
  TST101: SCOPE

  :/MAKE SURE CLOCK IS CLEAR.
  :/CLEAR THE BUFFER.
  :/SELECT: MODE 0, RATE 100KHZ ; GO.

  CLR $GDDAT
  ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
  ;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
  MOV #14,$GDDAT
  ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
  CLR R0 ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
  1$: INC R0 ;/WILL AMOUNT TO 369MS ON A PDP-11/20
  BNE 1$ ;/DID COUNTER INCREMENT AT ALL?

  ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
  TST $BDDAT
  BNE 2$ ;/IF YES - BR NEXT TEST.

  ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.

  ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
  BIT #BIT05,$BDDAT
  ;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'
  ;/F/F HAD SET.
  BNE 2$ ;/BR IF YES NEXT TEST.

  :;:*****>> ERROR <<*****

  ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
  ;/COUNT RATE: 100KHZ.

  :;:*****>> ERROR <<*****

  2$:
  
```


2284
(1)
(5)
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(1)
(2)

012530 000004

:/#

*TEST 103 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
*
*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
*IN RATE: 1KHZ PART 1
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*

TST103: SCOPE

012532 005037 001124

:/MAKE SURE CLOCK IS CLEAR.
:/CLEAR THE BUFFER.
:/SELECT: MODE 0, RATE 1KHZ ; GO.

CLR \$GDDAT
;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

012556 012737 000011 001124

;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
;* MOV \$GDDAT,@ABR
MOV #1!10,\$GDDAT

012574 005000
012576 005200
012600 001376

;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
* MOV \$GDDAT,@ASR ;/ NOW WE'LL DO A LITTLE DELAY: THIS DELAY
CLR R0 ;/ WILL AMOUNT TO 369MS ON A PDP-11/20
1\$: INC R0
BNE 1\$;/ DID COUNTER INCREMENT AT ALL?

012612 005737 001126
012616 001011

;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
;* MOV @ACR,\$BDDAT ;/ IF YES - BR NEXT TEST.
TST \$BDDAT
BNE 2\$;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.

012630 032737 000040 001126

;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
;* MOV @ASR,\$BDDAT ;/ AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'
BIT #BIT05,\$BDDAT ;/ F/F HAD SET.
BNE 2\$;/ BR IF YES NEXT TEST.

012636 001001

::: \$ ERROR << \$

012640 104012

ERROR 12 ;/ ERROR CLOCK A COUNTER FAILED TO
;/COUNT RATE: 1KHZ.

::: \$ ERROR << \$

012642

2\$:

2285
(1)
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(4)
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(5)
(6)
(6)
(6)
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(4)
(3) 012642 000004
(1)
(1)
(1)
(1)
(1) 012644 005037 001124
(2)
(2)
(2)
(2) 012670 012737 000013 001124
(2)
(2)
(1) 012706 005000
(1) 012710 005200
(1) 012712 001376
(1)
(2)
(2)
(1) 012724 005737 001126
(1) 012730 001011
(1)
(1)
(2)
(2)
(1) 012742 032737 000040 001126
(1)
(1)
(1) 012750 001001
(2)
(1) 012752 104012
(1)
(2)
(1) 012754

```
;/#  
:*****  
*TEST 104 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1  
*  
*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT  
*IN RATE: 100HZ PART 1  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'  
*  
:*****  
TST104: SCOPE  
:/MAKE SURE CLOCK IS CLEAR.  
:/CLEAR THE BUFFER.  
:/SELECT: MODE 0, RATE 100HZ ; GO.  
CLR $GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
MOV #1:12,$GDDAT  
;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY  
1$: INC R0 ;/WILL AMOUNT TO 369MS ON A PDP-11/20  
BNE 1$ ;/DID COUNTER INCREMENT AT ALL?  
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
TST $BDDAT ;/IF YES - BR NEXT TEST.  
BNE 2$ ;/COUNTER MAY HAVE HAD TIME TO OVERFLOW.  
;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
BIT #BIT05,$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF 'OVERFLOW'  
; /F/F HAD SET.  
BNE 2$ ;/BR IF YES NEXT TEST.  
:;:*****>> ERROR <<*****  
ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO  
; /COUNT RATE: 100HZ.  
:;:*****>> ERROR <<*****  
2$:
```


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(5)
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2301
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(1)
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2318
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2320
2321

013066 000004

013070 005037 001124

013114 005237 001124

013130 005000
013132 005200
013134 001376

013146 005737 001126
013152 001010

013164 032737 000040 001126

013172 001401

013174 104012

013176

 ;*ITS RATES, SO LETS BE SURE IT DOESNT
 ;*COUNT WHEN NO RATE IS SELECTED. ON
 ;*ERROR SUSPECT DUAL RATE SELECTION.
 ;*
 ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
 ;*

 TST106: SCOPE

```

                ;CLEAR CLOCK A.
                ;ZERO ITS BUFFER.
                ;TELL THE CLOCK TO GO!
                CLR    $GDDAT
    ;*          MOV    $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
    ;*          MOV    $GDDAT,@ABR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
                INC    $GDDAT
    ;*          MOV    $GDDAT,@ASR    ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
                ;NO RATE SELECTED.
1$:             CLR    RO
                INC    RO
                BNE    1$
                ;ANY COUNT OCCUR?
    ;*          MOV    @ACR,$BDDAT   ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
                TST    $BDDAT
                BNE    2$
                ;IF COUNTER HAS SOMETHING IN IT REPORT ERROR
    ;*          MOV    @ASR,$BDDA1  ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
                BIT    #BIT05,$BDDAT ;IF THE OVERFLOW BIT SET THEN IT MUST
                ;HAVE COUNTED.
                BEQ    3$
    
```

:::\$>> ERROR <<\$

```

2$:           ERROR    12           ;AH HA! ERROR CLOCK A COUNTED WHEN
                ;ENABLED-BUT-NO-RATE SELECTED
                ;BETTER FIND OUT HOW CAUSED SIGNAL:
                ;"CLOCK A" L.
    
```

:::\$>> ERROR <<\$

3\$:

 ;*TEST 107 *TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
 ;*
 ;*IN THIS TEST WE'LL FIND OUT IF F/F 'ENB CNTR A' WHEN SET.
 ;*INHIBITS LOADING OF CLOCK A'S COUNT REGISTER
 ;*THE LOADING OF THE COUNT REGISTER IS A FUNCTION OF:
 ;*'ENB CNTR (0)' H + 'BUFFER LOAD' H

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(4)
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(5)
(3)
(2) 013176 000004

:*
:PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'
:*****
TST107: SCOPE

2340
2341 ;GENERATE A SYNC PULSE
2342 ;CLEAR CLOCK A'S STATUS REG.
2343 ;CLEAR CLOCK A'S BUFFER REG. NOTE
2344 ;THIS WILL ALSO CAUSE ZEROS TO BE
2345 ;LOADED INTO THE COUNT REG.
2346

(1) ;* MOV @BSR,\$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$BDDAT.
2347 013210 005737 001126 TST \$BDDAT
2348 013214 005037 001124 CLR \$GDDAT

(1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2350

(1) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
2351 013240 005237 001124 INC \$GDDAT ;SET THE ENABLE F/F. THIS

(1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2353 FROM BEING LOADED WHEN THE
2354 BUFFER IS LOADED.

2355 013254 012737 177777 001124 MOV #177777,\$GDDAT ;NOW LOAD THE BUFFER REG.

(1) ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
2357 TO THE COUNT REGISTER.
2358 ;DID ANY BITS GET TRANSFERRED TO
2359 ;THE COUNT REGISTER?
2360

(1) ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
2361 013302 005737 001126 TST \$BDDAT
2362 013306 001401 BEQ 1\$;BR IF NO - NEXT TEST.
2363

:::\$>> ERROR <<\$

2364 013310 104012 ERROR 12 ;ERROR CLOCK A BUFFER TO COUNT REG TRANSFER
2365 OCCURRED EVEN THOUGH THE 'ENB CNTR A' F/F
2366 WAS SET.
2367

:::\$>> ERROR <<\$

2368 013312 1\$:

2369
2378 :*****
2379 :*TEST 110 *TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
(3)
(4)
(4) ;*NOW WE'RE GOING TO SEE IF 'A OVERFLOW' H WHEN GENERATED
(4) ;*BY CAUSING AN OVERFLOW DOESN'T CLEAR THE 'ENB CNTR A' F/F
(4) ;*WHEN IN MODE 1. IF F/F GETS CLEARED SUSPECT SIGNAL 'MODE 0' H.
(4)
(5)
(5) :* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'

(5)
(3)
(2) 013312 000004

2380
2381
2382
2383
2384
2385
2386
2387
2388

TST110: SCOPE

MAKE SURE CLOCK A IS CLEAR.
SET BUFFER + COUNT REG. TO -1 FROM OVERFLOW
SET: MODE 1; RATE STP1; GO.
CAUSE A MAINTENANCE STP4. CLOCK 1
SHOULD OVERFLOW - BUT THIS OVERFLOW SHOULD
NOT CLEAR 'ENB CNTR A' F/F.
DID BIT00, 'ENB CNTR A' F/F GET CLEARED?

013314 005037 001124

CLR \$GDDAT

(1) 013330 012737 177777 001124

MOV \$GDDAT,@ASR ;/
MOV #177777,\$GDDAT

PUT DATA FROM \$GDDAT TO DEVICE REG ASR

(1) 013346 012737 000415 001124

MOV \$GDDAT,@ABR ;/
MOV #415,\$GDDAT

PUT DATA FROM \$GDDAT TO DEVICE REG ABR

(1) 013374 052737 010000 001354

MOV \$GDDAT,@ASR ;/
BIS #BIT12,\$TMDAT

PUT DATA FROM \$GDDAT TO DEVICE REG ASR
/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.

(1) 013422 032737 000001 001126

MOV \$TMDAT,@ASR ;/
BIT #BIT00,\$BDDAT

PUT DATA FROM \$TMDAT TO DEVICE REG ASR
/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.

(1) 013430 001001

BNE 1\$

BR IF NO TO NEXT TEST.

ERROR <<*****

013432 104012

ERROR 12

ERROR MODE 1 OPERATION 'ENB CNTR A' F/F
WAS CLEARED ON OVERFLOW.

ERROR <<*****

013434

1\$:

2405
2417
2418

*TEST 111 *TEST THAT A CLOCK A 'BUFFER TO COUNT REG' DOESN'T TAKE PLACE ON A MODE
*THIS WILL BE THE FIRST TIME WE'VE DONE A MODE 2 OPERATION
*ON CLOCK A. THE FUNCTION OF THIS TEST WILL BE TO MAKE
*SURE A BUFFER TO COUNT REGISTER DOESN'T TAKE PLACE ON OVERFLOW
*THE COMBO THAT GAVE US BUFFER TO COUNT REG ON OVERFLOW BEFORE
*IS ['MODE A1 (0)' H + 'A RELOAD' H]. WE'LL STILL BE GENERATING
*PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
* 'A RELOAD' H BUT SHOULD NOT GET.'MODE A1 (0)' H AS THIS IS MODE 2.

TST111: SCOPE

(3) 013434 000004

(4)

(4)

(4)

(4)

(3) 013434 000004
2419

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 2425
 2426
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 (1)
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 (1)
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 (1)
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 (1)
 2435
 2436
 (1)
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 (1)
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 2440

013436 005037 001124
 013452 012737 177777 001124
 013470 012737 001015 001124
 013516 052737 010000 001124
 013544 005737 001126
 013550 001401
 104012
 013554

CLR \$GDDAT
 :* MOV \$GDDAT,@ASR
 MOV #177777,\$GDDAT
 :* MOV \$GDDAT,@ABR
 MOV #1015,\$GDDAT
 :* MOV \$GDDAT,@ASR
 :* MOV @ASR,\$GDDAT
 BIS #BIT12,\$GDDAT
 :* MOV \$GDDAT,@ASR
 :* MOV @ACR,\$BDDAT
 TST \$BDDAT
 BEQ 18

;MAKE SURE CLOCK A IS CLEAR.
 ;SET BUFFER + COUNT REG TO -1 FROM OVERFLOW.
 ;SET: MODE 2; RATE STP1; GO.
 ;CAUSE A MAINTENANCE STP1 - CLOCK ONCE.
 ;THIS SHOULD CAUSE AN OVERFLOW AND LEAVE
 ;THE COUNT REGISTER CLEAR AS A
 ;BUFFER TO COUNT REG. SHOULDN'T OCCUR.
 ;IS THE COUNT REG. CLEAR?
 ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
 ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
 ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
 ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
 ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
 ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
 ;BR IF YES TO NEXT TEST.

::: \$>> ERROR << \$

;ERROR THE CONTENTS OF THE BUFFER REG.
 ;GOT TRANSFERRED TO THE COUNT REG.
 ;(CLOCK A) ON OVERFLOW DOING A
 ;MODE 2 OPERATION.
 ;THERE'S AN OUTSIDE CHANCE THAT THE
 ;COUNT REG. NEVER GOES TO ZERO ON
 ;AN OVERFLOW - THIS IS THE FIRST TIME
 ;THAT WE WERE ABLE TO LOOK AT IT ON
 ;OVERFLOW BECAUSE MODES 0 + 1 CAUSED
 ;THAT AUTOMATIC BUFFER TO COUNT REG.

::: \$>> ERROR << \$

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 2454
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 (5)

013554
 18:

 *TEST 112 *TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
 ;*
 ;*NOW WE'LL SEE IF CAN GENERATE A 'CNTR TO BUFF' H SIGNAL.
 ;*TO DETECT IT, WE'RE GOING TO DEPEND ON IT SETTING THE MODE FLAG,
 ;*CLOCK A CSR BIT07. ['MODE A1 (0)' H + 'ST2 (1)' H] + 'TPO' L='CNTR TO BUFF' H.
 ;*BEING IN MODE 2, SHOULD GIVE US 'MODE A1 (1)' H. WELL GET ST2 (1) H
 ;*BY GENERATING A MAINTENANCE 'ST2'. TPO COMES FROM THE INTERNAL
 ;*CLOCK PAGE.
 ;*


```
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(3) 013674 000004
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(2) 013706 005737 001126
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(1)
(1) 013712 005037 001124
(2)
(2) 013726 012737 052525 001124
(1)
(2)
(2) 013744 012737 001001 001124
(1)
(2)
(2) 013762 005037 001124
(1)
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(2)
(2) 014006 052737 002000 001124
(1)
(2)
(1) 014024 012737 052525 001124
(1)
(1)
(2)
(2) 014042 023737 001126 001124
(1) 014050 001401
(2)
    ::=:*****>> ERROR <<*****
(1) 014052 104012
(1)
(1)
(1)
(2)
    ::=:*****>> ERROR <<*****
(1) 014054
(1) 000011
2549
(5)
(4)
(5)
; *
; * PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'
; *
; * *****
TST113: SCOPE
; GENERATE A SYNC PULSE
; *
; * MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
; * TST $BDDAT
; *
; * MAKE SURE CLOCK A IS CLEAR.
; * PUT PATTERN 052525 INTO BUFFER REG.
; * IT SHOULD GET XFERRED TO COUNT REG.
; * SELECT: MODE 2, ENABLE.
; * NOW GENERATE A MAINTENANCE ST2.
CLR $GDDAT
; *
; * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV #052525,$GDDAT
; *
; * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
; * MOV #1001,$GDDAT
; *
; * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * CLR $GDDAT
; *
; * MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
; *
; * MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
; * BIS #BIT10,$GDDAT
; *
; * MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV #052525,$GDDAT ;RECORD $GDDAT (PATTERN) IN CASE WE
; * NEED TO TYPE OUT AN ERROR.
; * NOW READ BACK THE BUFFER REG.
; *
; * MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
; * CMP $BDDAT,$GDDAT ;WAS THE TRANSFER SUCCESSFUL?
; * BEQ 1$ ;IF YES THEN BR TO NEXT TEST.
    ::=:*****>> ERROR <<*****
    ERROR 12 ;ERROR FAILED TO XFERR 052525 PATTERN
    ;CORRECTLY FROM COUNT TO BUFFER REG.
    ;SEE INIT. COMMENT AS TO WHY
    ;IT MIGHT HAVE GONE SOUR.
    ::=:*****>> ERROR <<*****
1$:
    P=P+1
; * *****
; * TEST 114 *TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
; *
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```

:*NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE
:*CAN GENERATE "CNTR TO BUFF" H FROM MODE 2 + MAINTENANCE ST2, NOW
:*WE WILL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER
:*USING A CB PAT PATTERN.
:*IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG 'LD BUFFER'
:*TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR
:*"CNTR TO BUFF" H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE
:*BUFFER REGISTER.
:*IF JUST ONE OR A FEW BITS GETS MESSED UP ON THE XFERR-
:*SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG
:*AND MUX. GOOD LUCK.
:*
:* PROBABLE SYNC POINT FOR THIS TEST:: 'RD STAT B'

```

014054 000004

TST114: SCOPE


```

;GENERATE A SYNC PULSE
:* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
   TST $BDDAT
;MAKE SURE CLOCK A IS CLEAR.
;PUT PATTERN 125252 INTO BUFFER REG.
;IT SHOULD GET XFERRERD TO COUNT REG.
;SELECT: MODE 2, ENABLE.
;NOW GENERATE A MAINTENANCE ST2.
   CLR $GDDAT
:* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
   MOV #125252,$GDDAT
:* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
   MOV #1001,$GDDAT
:* MOV $GDDAT,@ASR ;/ PUT DATA ROM $GDDAT TO DEVICE REG ASR
   CLR $GDDAT
:* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
:* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
   BIS #BIT10,$GDDAT
:* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
   MOV #125252,$GDDAT ;RECORD $GDDAT (PATTERN) IN CASE WE
                        ;NEED TO TYPE OUT AN ERROR.
                        ;NOW READ BACK THE BUFFER REG.
:* MOV @ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
   CMP $BDDAT,$GDDAT ;WAS THE TRANSFER SUCCESSFUL?
   BEQ 1$ ;IF YES THEN BR TO NEXT TEST.

```

;;;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSSSS

014232 104012

ERROR 12

;ERROR FAILED TO XFERR 125252 PATTERN
 ;CORRECTLY FROM COUNT TO BUFFER REG.

;SEE INIT. COMMENT AS TO WHY
;IT MIGHT HAVE GONE SOUR.

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS

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(1) 014234
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(1) 014352
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(1)
(2)

(1)
2594

014234 000012 1\$:

P=P+1

:::*****
*TEST 115 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENER
*THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT
*REGISTER IN MODE 1 WHEN AN STP2 IS GENERATED.
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'

TST115: SCOPE

;MAKE SURE CLOCK A IS CLEAR.
;LOAD ALL ONES INTO BUFFER COUNT REGS.
;SET MODE 1.
;GENERATE A MAINTENANCE STP2.
;SEE IF IT CLEARED COUNT REG.

014236 005037 001124

CLR \$GDDAT

014252 012737 177777 001124

;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
MOV #177777,\$GDDAT

014270 012737 000200 001124

;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
MOV #200,\$GDDAT

014316 052737 002000 001124

;* MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
BIS #BIT10,\$GDDAT

014344 005737 001126

;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
TST \$BDDAT

014350 001001

BNE 1\$;BR IF NO - NEXT TEST.

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS

014352 104012

ERROR 12 ;ERROR CLOCK A MODE 1 + STP2 CLEARED COUNT REG.
;TO SCOPE FIND OUT WHAT IS GENERATING
;SIGNAL ON CLR INPUT OF COUNT REG.

:::SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS

014354 1\$:

(5) :*****
(4) :*TEST 116 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENER
(5) :*
(5) :*THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT
(5) :*REGISTER IN MODE 2 WHEN AN STP2 IS GENERATED.
(6) :*
(6) :* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(6) :*
(5) :*
(4) :*****
(3) 014354 000004 TST116: SCOPE

(1) ;MAKE SURE CLOCK A IS CLEAR.
(1) ;LOAD ALL ONES INTO BUFFER COUNT REGS.
(1) ;SET MODE 2.
(1) ;GENERATE A MAINTENANCE STP2.
(1) ;SEE IF IT CLEARED COUNT REG.
(1) 014356 005037 001124 CLR \$GDDAT
(2) ;
(2) * MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(1) 014372 012737 177777 001124 * MOV #177777,\$GDDAT
(2) ;
(2) * MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
(1) 014410 012737 001000 001124 * MOV #1000,\$GDDAT
(2) ;
(2) * MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) ;
(2) * MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
(1) 014436 052737 002000 001124 * BIS #BIT10,\$GDDAT
(2) ;
(2) * MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
(2) ;
(2) * MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
(1) 014464 005737 001126 * TST \$BDDAT
(1) 014470 001001 * BNE 1\$;BR IF NO - NEXT TEST.
(2) ;

:::*****>> ERROR <<*****
(1) 014472 104012 ERROR 12 ;ERROR CLOCK A MODE 2 + STP2 CLEARED COUNT REG.
(1) ;TO SCOPE FIND OUT WHAT IS GENERATING
(1) ;SIGNAL ON CLR INPUT OF COUNT REG.
(2) :::*****>> ERROR <<*****

(1) 014474 1\$:
(1) 2595 :*****
(1) 2606 :*TEST 117 *TEST THAT MODE 3 + "STP2" CLEARS A'S COUNT REGISTER.
(1) 2607 :*
(3) :*IN THIS TEST WE'LL DO A MODE 3 FOR THE FIRST TIME.
(4) :*MODE 3 + "STP2" SHOULD CLEAR THE COUNT REGISTER.
(4) :*WE KNOW FROM A PREVIOUS TEST THAT "INIT" L WAS ABLE TO
(4) :*CLEAR THE REG. AND ALSO THAT WE CAN GENERATE AN "STP2" H.
(4) :*'MODE A0 (1)" H + "MODE A1 (1)" H + "STP2" H = CLEARING SIGNAL .
(4) :*
(5) :*

(5)
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(2) 014474 000004
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2609
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2615 014476 012737 001400 001124
2616
(1)
2617 014514 012737 177777 001124
2618
(1)
2619
(1)
2620 014542 052737 002000 001124
2621
(1)
2622
(1)
2623 014570 005737 001126
2624 014574 001401
2625

```
; * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
; *
; *
; * *****
TST117: SCOPE

; CLEAR CLOCK A + SELECT MODE 3.
; LOAD ALL ONE'S TO BUFFER + COUNTER REGS.
; GENERATE A MAINTENANCE 'STP2'.
; THIS SHOULD CLEAR THE COUNT REG.

; IS COUNT REG. CLEAR?
MOV #1400,$GDDAT
; * MOV $GDDAT,@ASR ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
MOV #177777,$GDDAT
; * MOV $GDDAT,@ABR ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
; * MOV @ASR,$GDDAT ; / READ DEVICE REG ASR, PUT DATA IN $GDDAT.
BIS #BIT10,$GDDAT
; * MOV $GDDAT,@ASR ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV @ACR,$BDDAT ; / READ DEVICE REG ACR, PUT DATA IN $BDDAT.
TST $BDDAT
BEQ 1$ ; BR IF YES - NEXT TEST.
```

::: \$>> ERROR << \$
2626 014576 104012 ERROR 12 ; ERROR-CLOCK A-COUNT REGISTER FAILED TO
2627 ; CLEAR IN MODE 3 ON 'STP2' PULSE.
2628
::: \$>> ERROR << \$

2629 014600
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```
1$:
; * *****
; * TEST 120 *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
; *
; * THIS IS GOING TO BE A BIGGIE-WITH TWO PARTS.
; * PART1: WE'RE LOADING THE BUFFER WITH ALL ONES; MODE 0; RATE STP1,
; * WITH 'AUTO INC (1)' SET (FOR FIRST TIME!). NOW WE'LL GENERATE
; * THE THING TO WATCH FOR IS THE EXPLOSIVE COMBO OF
; * 'MODE A0 (0)' H + 'MODE A1 (0)' H (MODE 0) + 'AUTO INC (1)' H +
; * 'A OVERFLOW' ALL FEEDING THE DOWN COUNT SIDE OF THE 74193 CHIP.
; * THE RESULTS SHOULD BE 177776.
; * PART2: IF PART 1 WAS SUCCESSFUL WE'LL LOOK TO SEE IF
; * THE COUNTER GOT LOADED WITH THE NEW VALUE 177776.
; * THE HANG-UP HERE IS THAT 'A OVERFLOW' FEEDS A ONE SHOT
; * THAT GENERATES 'A RELOAD' H. WE KNOW THAT WE CAN
; * GET 'A RELOAD' H BUT THE BIG TEST HERE IS SEEING IF THAT
; * ONE SHOT SPITS OUT 'A RELOAD' H TOO SOON TO CATCH THE BUFFER
; * WITH ITS PANTS DOWN AS ITS DECREMENTING ITSELF.
; *
```

(5)
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(5)
(3)
(2) 014600 000004

** PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
**
:*****
TST120: SCOPE

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014600 000004

014602 005037 001124

014626 012737 177777 001124

014644 012737 000020 001124

014662 012737 000015 001124

014710 052737 010000 001124

014726 012737 177776 001124

014744 023727 001126 177776

014752 001402

014754 104012

CLR \$GDDAT

;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR

;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

MOV #177777,\$GDDAT

;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR

MOV #20,\$GDDAT

;* MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR

MOV #15,\$GDDAT

;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

;* MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.

BIS #BIT12,\$GDDAT

;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

;PART 1 DID BUFFER GET DECREMENTED?

MOV #177776,\$GDDAT ;SET FOR ERROR TYPEOUT IF ANY.

;READ THE RESULTS OF THE BUFFER.

;* MOV @ABR,\$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN \$BDDAT.

CMP \$BDDAT,#177776 ;DID BUFFER DECREMENT TO 177776?

BEQ 1\$;BR IF YES TO PART 2

:::*****>> ERROR <<*****

ERROR 12

;ERROR-CLOCK A. AFTER AN OVERFLOW
;WITH AUTO INC ENABLED MODE 0, THE
;BUFFER REGISTER FAILED TO DOWN COUNT
;SEE ABOVE COMMENTS FOR SEQUENCE

```

2693                                ;OF EVENTS.
2694 014756 000411 BR 2$           ;IF ERROR ONLY LOOP ON PART 1.
2695
   :::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
2696 014760 1$: ;PART 2 DID NEW COUNT GET TRANSFERRED TO COUNT REGISTER?
2697                                ;READ THE COUNT REGISTER
2698
2699                                ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1)                                ;DID NEW VALUE OF THE BUFFER
2700 014770 023727 001126 177776 ;* MOV @ACR,$BDDAT ;REGISTER GET PROPERLY LOADED INTO
   CMP $BDDAT,#177776 ;THE COUNT REGISTER?
2701                                ;BR IF YES - NEXT TEST.
2702 014776 001401 BEQ 2$
2703
2704   :::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
2705 015000 104012 ERROR 12 ;ERROR CLOCK A. NEW CONTENTS OF
2706                                ;BUFFER REGISTER FAILED TO BE PROPERLY
2707                                ;LOADED INTO COUNT REGISTER AFTER
2708                                ;AUTO DECREMENT.
2709                                ;SEE ABOVE COMMENTS FOR SEQUENCE OF EVENTS.
2710
   :::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS
2711 015002 005037 001124 2$: ;CLEAR AUTO INC OPTION.
2712                                CLR $GDDAT
2713
2714 ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
(1)
2723
2724 :::*****
(3) ;*TEST 121 *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
(4) ;*
(4) ;*FOR THIS TEST, WE'LL TRY DISABLING THE 1 MHZ CLOCK. TO DO THIS,
(4) ;*WE'LL SET THE 'DISABLE OSC 1 MHZ', BIT 11 IN CLOCK B SR. THEN
(4) ;*COUNTED OR OVERFLOWED, IF SO ERROR.
(4) ;*THE UNKNOWN THING HERE IS BIT 11 SETTING THE DISABLE F/F THAT
(4) ;*GATES WITH THE 1 MHZ FREG TO PRODUCE 'A 1 MHZ CLK' L
(5) ;*
(5) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
(5) ;*
(3) ;:*****
(2) 015016 000004 TST121: SCOPE
2725                                ;CLEAR CLOCK A.
2726                                ;SET THE 'DISABLE OSC 1 MHZ' F/F.
2727                                ;CLEAR THE BUFFER + COUNT REGS.
2728                                ;START CLOCK: RATE 1 MHZ, MODE 0, GO.
2729
2730 015020 005037 001124 CLR $GDDAT
2731
(1) ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
2732 015034 012737 004000 001124 ;* MOV #BIT11,$GDDAT
2733
(1) ;* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
2734 015052 005037 001124 CLR $GDDAT
2735

```

(1) 2736 015066 012737 000003 001124 ;* MOV \$GDDAT,@ABR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR
2737 MOV #3,\$GDDAT
(1) 2738 015104 005000 ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
2739 015106 105200 ; CLR RO ;SHORT DELAY. WE ALLOW THIS DELAY TO
2740 015110 100376 1\$: INCB RO ;OCCUR. IF THE 1 MHZ CLOCK IS DISABLED
2741 BPL 1\$;NO CLOCKING OF CLOCK A WILL OCCUR.
2742 ;SEE SOMETHING IN THE COUNT REGISTERS
(1) 2743 015122 005737 001126 ;* MOV @ACR,\$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.
2744 015126 001007 ; TST \$BDDAT ;DOES COUNT REG HAVE ANYTHING IN IT?
2745 ; BNE 2\$;YES - REPORT ERROR!
(1) 2746 015140 105737 001126 ;* MOV @ASR,\$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$BDDAT.
2747 015144 100001 ; TSTB \$BDDAT
2748 ; BPL 3\$;NO - BR NEXT TEST - NO ERROR.
:::#####>> ERROR <<#####<<
2749 015146 104012 2\$: ERROR 12 ;ERROR - UNABLE TO DISABLE 1 MHZ CLK
2750 ; USING 'DISABLE OSC 1 MHZ' F/F
2751
:::#####>> ERROR <<#####<<
2752 ; CLEAR CLOCK A.
2753 015150 005037 001124 3\$: CLR \$GDDAT
2754 (1) ;* MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR

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(3)
(2)

015164 000004

:TEST 122 *TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
: *
:VERY FIRST TIME COUNTING WITH CLOCK B.
:WHAT WE'LL TRY AND DO IS COUNT IT FROM 0 TO 1.
:WE DO HAVE A PROBLEM HERE HOWEVER. WE CAN'T READ CLOCK B AS IT
:COUNTS AND THERE IS NO NICE WAY OF GENERATING A "CLOCK B" L PULSE.
:SO WE'RE GOING TO HAVE TO DO A COUPLE TRICKY THINGS: (1) DISABLE
:CLOCK A'S 1 MHZ CLOCK (WE DID THAT IN LAST TEST) SO THAT WE CAN
:GENERATE A MAINTENANCE 1 MHZ PULSE THROUGH CLOCK A (NEVER
:DID THAT BEFORE); (2) SET CLOCK B 'FEED B TO A' BIT 05 (NEVER DID THAT
:BEFORE EITHER) SO THAT WE CAN ROUTE 'A 1 MHZ' H TO MAKE
:'B 1 MHZ' L TO GIVE US "CLOCK B" L

: * PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'

TST122: SCOPE

2777
2778
2779
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(1)
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(1)
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(1)
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(1)
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(1)
2792
2793
(1)
2794
(1)
2795
2796
2797

015166 012737 004000 001124
015204 005037 001124
015230 052737 000043 001124
015256 052737 004000 001124
015304 005737 001126
015310 001001

MOV #BIT11,\$GDDAT ;CLEAR CLOCK B AND DISABLE 1MHZ OSC.
: * MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
: ;CLEAR B'S BUFFER + COUNT REGS.
: ;SELECT 'FEED B TO A', RATE 1 MHZ, GO.
CLR \$GDDAT
: * MOV \$GDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
: ;CLOCK A'S 1 MHZ CLOCK.
: ;GENERATE A MAINTENANCE 1 MHZ PULSE..
: ;DID COUNTER COUNT?
: * MOV @BSR,\$GDDAT ;/READ DEVICE REG BSR,PUT DATA IN \$GDDAT.
: BIS #BIT5!BIT1!BIT0,\$GDDAT
: * MOV \$GDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
: * MOV @ASR,\$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.
: BIS #BIT11,\$GDDAT
: * MOV \$GDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
: * MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
: TST \$BDDAT
: BNE 1\$;BR IF YES TO NEXT TEST.

:::\$>> ERROR <<\$

2798
2799

015312 104014

ERROR 14

;ERROR - CLOCK B. FAILED TO ADVANCE
;COUNT REGISTER.

C 10

```

2848
(1)
2849 015402 005237 001354 ;*   MOV   $TMDAT,@BSR   ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
INC   $TMDAT
2850
(1)
2851 015416 ;*   MOV   $TMDAT,@BSR   ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
2852    2$:              ;GENERATE A CLOCK PULSE.
2853              ;SHOULD CAUSE THE CLOCK TO
2854              ;INCREMENT ONCE.
2855
(1)
2856 015426 052737 004000 001354 ;*   MOV   @ASR,$TMDAT   ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS   #BIT11,$TMDAT
2857
(1)
2858 015444 005237 001124 ;*   MOV   $TMDAT,@ASR   ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
INC   $GDDAT          ;$GDDAT IS USED TO KEEP TRACK OF THE
              ;VALUE THE CLOCK SHOULD COUNT TO.
2859
2860
2861
(1)
2862 ;*   MOV   @BCR,$BDDAT   ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
2863 015460 123737 001126 001124   CMPB   $BDDAT,$GDDAT   ;DID THE COUNT OCCUR CORRECTLY?
2864 015466 001402               BEQ   3$               ;IF YES - BR '3$'.
2865
  ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
2866 015470 104015               ERROR 15                ;ERROR CLOCK B FAILED TO UPCOUNT
2867                                          ;CORRECTLY - SEE COMMENTS AT SUB-TEST
2868                                          ;HEADING FOR MORE DETAILS.
2869
  ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR <<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

2870 015472 000403               BR    4$
2871
2872 015474 105737 001124           3$:   TSTB   $GDDAT          ;DID WE ACHIEVE OVERFLOW YET?
2873 015500 001410               BEQ   5$
2874
2875 015502 032777 040000 163430 4$:   BIT   #BIT14,@SWR     ;LOOP ON CURRENT COUNT?
2876 015510 001742               BEQ   2$               ;BR IF NO TO NEXT COUNT UPDATE.
2877 015512 162737 000001 001124   SUB   #1,$GDDAT       ;IF YES DECREMENT EXPECTED AND RELOAD.
2878 015520 000700               BR    1$               ;GO TO RELOAD POINT
2879
2880 015522           5$:              ;END SUBTEST.
2881
2882
2893
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(5)
(5)
(5)
(4)
    ;*****
    ;*TEST 124 *TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
    ;*
    ;*NOW WE'LL TRY AND GENERATE 'B OVERFLOW' L WHICH SETS BIT 07.
    ;*WE'LL DO IT BY PRESETTING THE BUFFER TO 377 AND GENERATING A 'CLOCK B' L
    ;*WE ALREADY KNOW WE CAN ADVANCE THE COUNTER, WHAT WE
    ;*WANT TO SEE IS 'B OVERFLOW' L COME OVER AND DIRECT SET
    ;*'OVERFLOW FL B' F/F (BIT 07 IN CSR).
    ;*
    ;*
    ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'
    ;*
    ;*
    ;*
  
```


::: \$ >> ERROR << \$

2933 015712 2\$:

2934
2942
2943
(3)
(4)
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(4)
(5)
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(5)
(4)
(3)

: *TEST 125 *TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.
: *
: *ALL WE'RE GOING TO DO HERE IS TEST THE INITIALIZE INPUTS
: *TO THE 74193 ICS THAT FORM THE COUNT REGISTER.
: *
: * PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'
: *
: *

TST125: SCOPE

(2) 015712 000004

2944
2945
2946
2947
2948 015714 005037 001124
2949
(1)
2950

:CLEAR CLOCK A.
:CLEAR CLOCK B.
:LOAD ALL ONES TO BUFFER + COUNT REGS.

CLR SGDDAT
: * MOV SGDDAT,@ASR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG ASR
: * MOV SGDDAT,@BSR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BSR
MOV #377,\$GDDAT

2951 015740 012737 000377 001124
2952
(1)
2953

: * MOV SGDDAT,@BBR ;/ PUT DATA FROM \$GDDAT TO DEVICE REG BBR
JSR PC,\$RESET ;DO SYSTEM INIT - GENERATES "INIT" H.

2954 015756 004737 032534
2955
2956 015762 005037 001124
2957
2958
(1)
2959 015776 005737 001126
2960
2961 016002 001401
2962

CLR SGDDAT ;FIX \$GDDAT FOR ERROR TYPEOUT, IF NEEDED.
;READ B'S COUNT REGISTER, INIT

: * MOV @BCR,\$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN \$BDDAT.
TST \$BDDAT
;SHOULD HAVE MADE IT AL ZEROS.
BEQ 1\$;BR IF YES - NEXT TEST.

::: \$ >> ERROR << \$

2963 016004 104007 ERROR 7
2964
2965

;ERROR CLOCK B - INIT FAILED TO CLEAR
;COUNT REG.

::: \$ >> ERROR << \$

2966 016006 1\$:

3049
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016226 000004

016230 005037 001124

016264 012737 000005 001124

016302 005000
016304 005200
016306 001376

016320 005737 001126
016324 001010

016336 105737 001126

016342 100401

016344 104014

016346

```

;/#
*****
*TEST 130    *TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
*
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*IN RATE: 100KHZ    PART1
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'
*
*****
TST130: SCOPE

```

```

; /CLEAR CLOCK A.
CLR    $GDDAT
; /CLEAR CLOCK B.
; /CLEAR THE BUFFER + COUNT REGS.
; /SELECT: RATE: 100KHZ ; GO.
; *
; * MOV    $GDDAT,@ASR    ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV    $GDDAT,@BSR    ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
; * MOV    $GDDAT,@BBR    ; / PUT DATA FROM $GDDAT TO DEVICE REG BBR
MOV    #1!4,$GDDAT
; * MOV    $GDDAT,@BSR    ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
CLR    R0
; /NOW WE'LL DO A LITTLE DELAY.
INC    R0
; /THIS DELAY WILL AMOUNT TO APP. 269 MS.
BNE    1$
; /ON A PDP-11/20.
; /DID COUNTER COUNT AT ALL?
; * MOV    @BCR,$BDDAT    ; /READ DEVICE REG BCR,PUT DATA IN $BDDAT.
TST    $BDDAT
BNE    2$
; /BR IF YES - NEXT TEST.
; * MOV    @BSR,$BDDAT    ; /READ DEVICE REG BSR,PUT DATA IN $BDDAT.
TSTB   $BDDAT
; /COUNT TO OVERFLOW - SO WE'LL SEE IF
; /THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
BMI    2$
; /BR IF SET - NEXT TEST.
:::#####>> ERROR <<#####
ERROR  14
; /ERROR CLOCK B - COUNTER FAILED TO COUNT
; /AT 100KHZ RATE.
:::#####>> ERROR <<#####
2$:

```

3050

(1)
(5)
(4)
(5)
(5)
(5)
(6)
(6)
(6)
(5)
(4)

```
;/#  
:*****  
:*TEST 131 *TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1  
:*  
:*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  
:*IN RATE: 10KHZ PART1  
:*  
:* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT A'  
:*  
:*****  
TST131: SCOPE
```

(3) 016346 000004
(1)
(1)
(1) 016350 005037 001124
(1)
(1)
(1)
(1)
(2)
(2)
(2)
(2)
(2)
(1) 016404 012737 000007 001124
(2)
(2)
(1)
(1) 016422 005000
(1) 016424 005200
(1) 016426 001376
(1)
(1)
(2)
(2)
(1) 016440 005737 001126
(1) 016444 001010
(1)
(2)
(2)
(1) 016456 105737 001126
(1)
(1)
(1) 016462 100401
(2)

```
;/CLEAR CLOCK A.  
CLR $GDDAT  
;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: 10KHZ ; GO.  
:* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
:* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
:* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #1!6,$GDDAT  
:* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.  
1$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  
BNE 1$ ;/ON A PDP-11/20.  
;/DID COUNTER COUNT AT ALL?  
:* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/BR IF YES - NEXT TEST.  
:* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TSTB $BDDAT  
;/COUNT TO OVERFLOW - SO WE'LL SEE IF  
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  
BMI 2$ ;/BR IF SET - NEXT TEST.
```

:::*****>> ERROR <<*****

(1) 016464 104014
(1)
(2)

```
ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
;/AT 10KHZ RATE.
```

:::*****>> ERROR <<*****

(1) 016466

2\$:

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(4)
(4)
(4)
(4)
(5)
(5)
(5)
(4)
(3)
(2)
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3098

017046 000004

017050 005037 001124

017104 012737 000377 001124

017122 012737 004042 001124

017140 005237 001124

017154 012737 000001 001124

017202 052737 004000 001124

017230 005737 001126

```
*****
*TEST 135 *TEST THE 'FEED B TO A' 24 BIT COUNTER FEATURE OF CLOCKS A + B
*
*WE'RE GOING TO TEST CLOCKS A+B AS A 24 BIT COUNTER; THAT IS;
*WE'RE GOING TO TAKE THE OVERFLOW FROM CLOCK B AND FEED IT INTO
*CLOCK A.
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF B'
*
*****
TST135: SCOPE
```

```
;CLEAR CLOCK A.
;CLEAR CLOCK B.
;CLEAR A'S BUFFER + COUNT REGISTERS.
;PRESET B'S BUFFER + COUNT TO -1 FROM
;OVERFLOW.
;SELECT: 'DISABLE OSC 1 MHZ'; RATE 1 MHZ;
;'FEED B TO A'
;SET ENABL. MUST BE SET AFTER 'FEED B TO A'.
;ENABLE CLOCK A; MODE 0; RATE 0.
;SIMULATE A 1 MHZ PULSE - THIS PULSE
;WILL CLOCK CLOCK B'S COUNTER
;REGISTER. AN OVERFLOW WILL
;OCCUR - THAT OVERFLOW SHOULD
;CLOCK CLOCK A'S COUNT REGISTER.
;DID CLOCK A'S COUNT REG GET CLOCKED?
```

```
* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
* MOV $GDDAT,@ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
  MOV #377,$GDDAT
* MOV $GDDAT,@BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
  MOV #4042,$GDDAT
* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
  INC $GDDAT
* MOV $GDDAT,@BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
  MOV #1,$GDDAT
* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
  BIS #BIT11,$GDDAT
* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
  TST $BDDAT
```

3099 017234 001001 BNE 18 ;IF YES THEN BR NEXT TEST.
3100

:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS

3101 017236 104014 ERROR 14 ;ERROR - UNABLE TO CLOCK CLOCK A'S
3102 ;COUNT REGISTER WITH THE OVERFLOW
3103 ;FROM CLOCK B.
3104 ;THE MOST LOGICAL PLACE TO START
3105 ;WOULD BE !A CLOCK TIMING"
3106 ;"FEED B TO A (1)" H + "B OVERFLOW" H
3107 ;SHOULD BE COMING TOGETHER GOING
3108 ;INTO THE MUX - BEGING SELECTED AND
3109 ;COMING OUT OF THE MUX TO BECOME
3110 ;"CLOCK A" L.
3111

:::SSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SSSSSSSSSSSSSSSSSSSSSSSSSS

3112 017240 iS:
3113 .SBTTL *
3114 .SBTTL * PHASE 6 CLOCK A+B ADVANCE TESTING
3115 .SBTTL *
3116

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;/#

```

:*****
:TEST 136      *TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER
:
:*IN THIS TEST WE'LL SEE IF WE CATCH THE FIRST COUNT
:*AFTER STP1 COMES IN AND SETS THE ENABLE F/F ('ST1 ENB COUNTER'
:*SET).
:*WHAT WE SHOULD SEE IS THE LEADING EDGE OF ST1 COME
:*IN AND SET THE ENB F/F AND THE TRAILING EDGE TRIGGER
:*A 'CLOCK A' PULSE TO INCREMENT THE COUNTER.
:*WE KNOW FROM A PREVIOUS TEST THAT AN STP1 WILL
:*COME IN AND SET 'ENABL CNTR A' F/F AND THAT THE
:*COUNTER WILL INCREMENT, SO WHATS HAPPENING IS WE'RE ACCUALLY
:*LOOKING AT THE TRAILING EDGE OF STP1 TO SEE IF ITS DOING
:*THE INCREMENTING
:
:*
:* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
:*****
:TST136: SCOPE

```

017240 000004

```

;CLR CLK A, SET 'ST1 ENB COUNTER'.;RATE:STP1.
;CLR COUNT + BUFFER REGS.
;GENERATE A MAINTENANCE ST1.
;THE LEADING EDGE SHOULD CAUSE
;'.ENABL CNTR A' F/F TO SET (CSR BIT 00).
;THE TRAILING EDGE SHOULD CLOCK
;THE COUNTER ONCE.

```

017242 012737 000001 001354

MOV #BIT0,\$TMDAT

017260 005037 001124

;* MOV \$TMDAT,@ASR
CLR \$GDDAT

;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR

017304 052737 010000 001124

;* MOV \$GDDAT,@ABR
BIS @ASR,\$GDDAT

;/ PUT DATA FROM \$GDDAT TO DEVICE REG ABR

017322 012737 000001 001124

MOV #1,\$GDDAT

;/READ DEVICE REG ASR,PUT DATA IN \$GDDAT.

017340 023737 001126 001124

;* MOV @ACR,\$BDDAT
CMP \$BDDAT,\$GDDAT

;/READ DEVICE REG ACR,PUT DATA IN \$BDDAT.

017346 001401

BEG 1\$

;/DID THE COUNT REG COUNT ONCE?

;/BR IF YES TO NEXT TEST.

::: \$ >> ERROR << \$

017350 104012

ERROR 12

```

;ST1 FAILED TO COUNT
;CLOCK A'S COUNT REG. AFTER SETTING
;'ENABL CNTR A' - SEE TEST HEADING

```

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; COMMENTS

:::XXXXXXXXXXXXXXXXXXXXXXXXXXXX>> ERROR <<XXXXXXXXXXXXXXXXXXXXXXXXXXXX

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(1) 017410 012737 004000 001354
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(2) 017436 052737 000405 001354
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(1) 017454 012700 177766
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(1) 017460
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(1) 017470 052737 004000 001354
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(1) 017516 005737 001126
(1) 017522 001002
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```

:/#
:*****
:*TEST 137 *TEST CLOCK A'S 100KHZ DIVIDER
*
*IN THIS TEST WE'LL SEE IF THE 100KHZ DIVIDER WILL DIVIDE 1MHZ
*BY 10 TO GIVE US A 100KHZ CLK L PULSE.
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100KHZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 1MHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 100KHZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*
:*****
TST137: SCOPE
: /CLEAR CLOCK B.
: /CLEAR CLOCK A.
: /CLEAR A'S BUFFER + COUNT REGS.
: /DISABLE THE 1MHZ OSC.
: /ENABLE CNTR, RATE: 100KHZ ;MODE.

CLR $TMDAT
:* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
:* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
:* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV #BIT11,$TMDAT
:* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
:* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #401!4,$TMDAT
:* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
: /SET TO GENERATE ON 1MHZ PULSES
MOV #-10.,R0
1$: ;/GENERATE 1 1MHZ PULSE
: /HAS COUNTER ADVANCED ANY?
:* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
:* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
:* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/IF SO EXIT THIS LOOP.
: /NOTE: WHEN WE DISABLED THE 1 MHZ.

```


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017642 000004

017644 005037 001354

017700 012737 004000 001354

017726 052737 000407 001354

017744 012700 177634

017750

017760 052737 004000 001354

020006 005737 001126

020012 001002

```
;/#
*****
*TEST 140 *TEST CLOCK A'S 10KHZ DIVIDER
*
*IN THIS TEST WE'LL SEE IF THE 10KHZ DIVIDER WILL DIVIDE 100KHZ
*BY 10 TO GIVE US A 10KHZ CLK L PULSE.
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 10KHZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 100KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 10KHZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*****
TST140: SCOPE
```

```
;/CLEAR CLOCK B.
;/CLEAR CLOCK A.
;/CLEAR A'S BUFFER + COUNT REGS.
;/DISABLE THE 1MHZ OSC.
;/ENABLE CNTR, RATE: 10KHZ ;MODE.
```

```
CLR $TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV #BIT11,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #401!6,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;/SET TO GENERATE ON 1MHZ PULSES
MOV #-100.,R0
1$: ;/GENERATE 1 1MHZ PULSE
;/HAS COUNTER ADVANCED ANY?
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/IF SO EXIT THIS LOOP.
;/NOTE: WHEN WE DISABLED THE 1 MHZ.
```

```

(1)                                     ;/OSC., THE DIVIDER COULD HAVE
(1)                                     ;/AND COUNT LEFT IN IT.
(1)                                     ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) 020014 005200                       INC     R0
(1) 020016 001354                       BNE     1$
(1)                                     ;/DONE 100. 1MHZ PULSES?
(1) 020020 012737 000001 001124 10$:   MOV     #1,$GDDAT
(1)                                     ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1)                                     ;/READ THE COUNTER.
(2)                                     ;*
(2)                                     MOV     @ACR,$BDDAT
(1)                                     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 020036 023737 001126 001124       CMP     $BDDAT,$GDDAT
(1) 020044 001402                       BEQ     2$
(2)                                     ;/DID THE COUNTER ADVANCE ONCE?
(2)                                     ;/IF YES - NEXT CHECK.
(2)                                     ;:::#####>> ERROR <<#####
(1) 020046 104012                       ERROR  12
(1)                                     ;/ERROR - CLOCK A - 10KHZ - PULSE
(2)                                     ;/NOT GENERATED WHEN 10 100KHZ PULSES
(2)                                     ;:::#####>> ERROR <<#####
(1) 020050 000430                       BR      4$
(1) 020052 012700 000143                2$:   MOV     #99.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1) 020056                                3$:   ;/GENERATE 9 100KHZ PULSES
(2)                                     ;*
(2) 020066 052737 004000 001354       MOV     @ASR,$TMDAT
(1)                                     BIS     #BIT11,$TMDAT
(2)                                     ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(2)                                     ;*
(2) 020104 005300                       MOV     $TMDAT,@ASR
(1) 020106 001363                       DEC     R0
(1)                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1)                                     ;/INORDER TO CHECK TO SEE THAT
(1)                                     ;/WE DON'T GENERATE ANOTHER 10KHZ PULSE.
(1)                                     ;/READ THE COUNTER
(2)                                     ;*
(2) 020120 023737 001126 001124       MOV     @ACR,$BDDAT
(1) 020126 001401                       CMP     $BDDAT,$GDDAT
(1)                                     BEQ     4$
(2)                                     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(2)                                     ;/WAS ANOTHER 10KHZ PULSE GENERATED?
(2)                                     ;/NO-GO TO NEXT TEST!
(2)                                     ;:::#####>> ERROR <<#####
(1) 020130 104012                       ERROR  12
(1)                                     ;/ERROR CLOCK A WE SEEM TO HAVE
(1)                                     ;/GENERATED A SECOND 10KHZ PULSE
(2)                                     ;/ON ONLY 9 100KHZ PULSES.
(2)                                     ;:::#####>> ERROR <<#####
(1) 020132                                4$:

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020132 000004

020134 005037 001354

020170 012737 004000 001354

020216 052737 000411 001354

020234 012700 176030

020240

020250 052737 004000 001354

020276 005737 001126

020302 001002

```

  ;/#
  :*****
  : *TEST 141 *TEST CLOCK A'S 1KHZ DIVIDER
  : *
  : *IN THIS TEST WE'LL SEE IF THE 1KHZ DIVIDER WILL DIVIDE 10KHZ
  : *BY 10 TO GIVE US A 1KHZ CLK L PULSE.
  : *TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
  : *PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 1KHZ
  : *PULSES.
  : *THEN WE'LL GENERATE 9 MORE 10KHZ PULSES AND MAKE
  : *SURE THAT WE DON'T GET ANOTHER 1KHZ PULSE.
  : *
  : *
  : * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
  : *
  :*****
  TST141: SCOPE

  ;/CLEAR CLOCK B.
  ;/CLEAR CLOCK A.
  ;/CLEAR A'S BUFFER + COUNT REGS.
  ;/DISABLE THE 1MHZ OSC.
  ;/ENABLE CNTR, RATE: 1KHZ ;MODE.

  CLR $TMDAT
  ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
  ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
  ;* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
  MOV #BIT11,$TMDAT
  ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
  ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
  BIS #401!10,$TMDAT
  ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASP
  ;/SET TO GENERATE ON 1MHZ PULSES

  MOV #-1000.,R0

  1$: ;/GENERATE 1 1MHZ PULSE
  ;/HAS COUNTER ADVANCED ANY?
  ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
  BIS #BIT11,$TMDAT
  ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
  ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
  TST $BDDAT
  BNE 10$
  ;/IF SO EXIT THIS LOOP.
  ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
  
```


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020422 000004

020424 005037 001354

020460 012737 004000 001354

020506 052737 000413 001354

020524 012700 154360

020530

020540 052737 004000 001354

020566 005737 001126

020572 001002

```

:/#
*****
*TEST 142      *TEST CLOCK A'S 100HZ DIVIDER
*
*IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
*BY 10 TO GIVE US A 100HZ CLK L PULSE.
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*****
TST142: SCOPE

```

```

:/CLEAR CLOCK B.
:/CLEAR CLOCK A.
:/CLEAR A'S BUFFER + COUNT REGS.
:/DISABLE THE 1MHZ OSC.
:/ENABLE CNTR, RATE: 100HZ ;MODE.

```

```

CLR      $TMDAT
;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;*      MOV      $TMDAT,@ABR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV      #BIT11,$TMDAT
MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS      #401!12,$TMDAT
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;/SET TO GENERATE ON 1MHZ PULSES
MOV      #-10000.,R0
1$:      ;/GENERATE 1 1MHZ PULSE
;/HAS COUNTER ADVANCED ANY?
;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS      #BIT11,$TMDAT
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST      $BDDAT
BNE      10$      ;/IF SO EXIT THIS LOOP.
;/NOTE: WHEN WE DISABLED THE 1 MHZ.

```

```
(1) ;/OSC.,THE DIVIDER COULD HAVE
(1) ;/AND COUNT LEFT IN IT.
(1) ;/AFTER THIS LOOP ,WE SHOULD BE SUNK.
(1) 020574 005200 INC R0
(1) 020576 001354 BNE 1$ ;/DONE 10000. 1MHZ PULSES?
(1) ;/IF NOT - DO ANOTHER.
(1) 020600 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1) ;/READ THE COUNTER.
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 020616 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
(1) 020624 001402 BEQ 2$ ;/IF YES - NEXT CHECK.
(2)
:::#####>> ERROR <<#####
(1) 020626 104012 ERROR 12 ;/ERROR - CLOCK A - 100HZ - PULSE
(1) ;/NOT GENERATED WHEN 10 1KHZ PULSES
(2)
:::#####>> ERROR <<#####
(1) 020630 000430 BR 4$
(1) 020632 012700 023417 2$: MOV #9999.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1) 020636 3$: ;/GENERATE 9 1KHZ PULSES
(2)
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 020646 052737 004000 001354 BIS #BIT11,$TMDAT
(2)
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 020664 005300 DEC R0 ;/INORDER TO CHECK TO SEE THAT
(1) 020666 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 100HZ PULSE.
(1) ;/READ THE COUNTER
(2)
(2) ;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
(1) 020700 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 100HZ PULSE GENERATED?
(1) 020706 001401 BEQ 4$ ;/NO-GO TO NEXT TEST!
(1)
(2)
:::#####>> ERROR <<#####
(1) 020710 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE
(1) ;/GENERATED A SECOND 100HZ PULSE
(1) ;/ON ONLY 9 1KHZ PULSES.
(2)
:::#####>> ERROR <<#####
(1) 020712 4$:
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(4) ;*TEST 143 *TEST CLOCK B'S 100KHZ DIVIDER
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020712 000004

020714 005037 001354

020750 012737 004040 001354

020776 052737 000004 001354

021014 005237 001354

021030 012700 177766

021034

021044 052737 004000 001354

021072 005737 001126
021076 001002

```

;* IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
;* BY 10 TO GIVE US A 100HZ CLK L PULSE.
;* TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
;* PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
;* PULSES.
;* THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
;* SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
;
;
; *
; *
; * PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
; *
; *
; *****
TST143: SCOPE

; /CLEAR CLOCK B.
; /CLEAR CLOCK A.

; /CLEAR B'S BUFFER + COUNT REGS.
; /DISABLE THE 1MHZ OSC.
; /RATE: 100KHZ
; /ENABLE CLOCK B.

CLR STMDAT

;* MOV STMDAT,@BSR ; / PUT DATA FROM STMDAT TO DEVICE REG BSR
;* MOV STMDAT,@ASR ; / PUT DATA FROM STMDAT TO DEVICE REG ASR
;* MOV STMDAT,@BBR ; / PUT DATA FROM STMDAT TO DEVICE REG BBR
MOV #BIT11!BITS,STMDAT

;* MOV STMDAT,@BSR ; / PUT DATA FROM STMDAT TO DEVICE REG BSR

;* MOV @BSR,STMDAT ; /READ DEVICE REG BSR,PUT DATA IN STMDAT.
BIS #4,STMDAT

;* MOV STMDAT,@BSR ; / PUT DATA FROM STMDAT TO DEVICE REG BSR
INC STMDAT

;* MOV STMDAT,@BSR ; / PUT DATA FROM STMDAT TO DEVICE REG BSR
MOV #-10.,R0 ; /SET TO GENERATE 10. 1MHZ PULSES

1$: ; /GENERATE 1 1MHZ PULSE
; /HAS THE COUNTER ADVANCED?

;* MOV @ASR,STMDAT ; /READ DEVICE REG ASR,PUT DATA IN STMDAT.
BIS #BIT11,STMDAT

;* MOV STMDAT,@ASR ; / PUT DATA FROM STMDAT TO DEVICE REG ASR

;* MOV @BCR,$BDDAT ; /READ DEVICE REG BCR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$

; /EXIT LOOP IF SO.
; /NOTE: WHEN WE DISABLED THE 1 MHZ.
; / OSC., THE DIVIDER COULD HAVE
; / HAD ANY COUNT IN IT.
; /AFTER THIS LOOP, WE SHOULD BE SUNK.
```



```
(1) (1) 021100 005200 INC R0 ;/DONE 10. 1MHZ PULSES?  
(1) (1) 021102 001354 BNE 1$ ;/IF NOT - DO ANOTHER.  
(1) (1) 021104 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.  
(1) (1) ;/READ THE COUNTER  
(2) (2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
(1) (1) 021122 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?  
(1) (1) 021130 001402 BEQ 2$ ;/IF YES - NEXT CHECK
```

:::*****>> ERROR <<*****

```
(1) (1) 021132 104015 ERROR 15 ;/ERROR - CLOCK B - 100KHZ - PULSE  
(1) (1) ;/NOT GENERATED WHEN 10 1MHZ PULSE  
(1) (1) ;/WERE GENERATED.
```

:::*****>> ERROR <<*****

```
(1) (1) 021134 000430 BR 4$  
(1) (1) 021136 012700 177767 2$: MOV #9.,R0 ;/GET THE NUMBER OF '1 MHZ'' H PULSES  
(1) (1) ;/NEED TO GIVE 9 1MHZ PULSES  
(1) (1) 021142 3$:  
(2) (2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) (1) 021152 052737 004000 001354 BIS #BIT11,$TMDAT  
(2) (2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(1) (1) 021170 005200 INC R0 ;/IN ORDER TO CHECK TO SEE THAT  
(1) (1) 021172 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 100KHZ PULSE
```

:::*****>> ERROR <<*****

```
(1) (1) 021214 104015 ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE  
(1) (1) ;/GENERATED A SECOND 100KHZ PULSE  
(1) (1) ;/ON ONLY 9 1MHZ PULSES.
```

:::*****>> ERROR <<*****

(1) 021216 4\$:
3363

```
(5) *****  
(4) ;*TEST 144 *TEST CLOCK B'S 10KHZ DIVIDER  
(5) ;*  
(5) ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ  
(5) ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.  
(5) ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
```

```

(5) ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
(5) ;*PULSES.
(5) ;*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
(5) ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
(5) ;*
(6) ;*
(6) ;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
(6) ;*
(4) ;*****
(3) 021216 000004 TST144: SCOPE
(1)
(1) ;/CLEAR CLOCK B.
(1) ;/CLEAR CLOCK A.
(1)
(1) ;/CLEAR B'S BUFFER + COUNT REGS.
(1) ;/DISABLE THE 1MHZ OSC.
(1) ;/RATE: 10KHZ
(1) ;/ENABLE CLOCK B.
(1) 021220 005037 001354 CLR $TMDAT
(2)
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
(1) 021254 012737 004040 001354 MOV #BIT11!BITS,$TMDAT
(2)
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(2) ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
(1) 021302 052737 000006 001354 BIS #6,$TMDAT
(2)
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 021320 005237 001354 INC $TMDAT
(2)
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1) 021334 012700 177634 MOV #-100.,R0 ;/SET TO GENERATE 100. 1MHZ PULSES
(1) 021340 1$: ;/GENERATE 1 1MHZ PULSE
(1) ;/HAS THE COUNTER ADVANCED?
(2)
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 021350 052737 004000 001354 BIS #BIT11,$TMDAT
(2)
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 021376 005737 001126 TST $BCDAT
(1) 021402 001002 BNE 1$ ;/EXIT LOOP IF SO.
(1) ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
(1) ;/ OSC., THE DIVIDER COULD HAVE
(1) ;/ HAD ANY COUNT IN IT.
(1) ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
(1) 021404 005200 INC R0 ;/DONE 100. 1MHZ PULSES?
(1) 021406 001354 BNE 1$ ;/IF NOT - DO ANOTHER.

```

```
(1) (1) 021410 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.  
(1) ;/READ THE COUNTER  
(1)  
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
(1)  
(1) 021426 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?  
(1) 021434 001402 BEQ 2$ ;/IF YES - NEXT CHECK  
(2)
```

:::*****>> ERROR <<*****

```
(1) 021436 104015 ERROR 15 ;/ERROR - CLOCK B - 10KHZ - PULSE  
(1) ;/NOT GENERATED WHEN 10 100KHZ PULSE  
(1) ;/WERE GENERATED.  
(2)
```

:::*****>> ERROR <<*****

```
(1) 021440 000430 BR 4$  
(1)  
(1) 021442 012700 177635 2$: MOV #-99.,R0 ;/GET THE NUMBER OF '1 MHZ' H PULSES  
(1) ;/NEED TO GIVE 9 100KHZ PULSES  
(1) 021446 3$:  
(2)
```

```
(2) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
(1) 021456 052737 004000 001354 BIS #BIT11,$TMDAT  
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
(1) 021474 005200 INC R0 ;/IN ORDER TO CHECK TO SEE THAT  
(1) 021476 001363 BNE 3$ ;/WE DON'T GENERATE ANOTHER 10KHZ PULSE  
(1)  
(2)
```

```
(1) 021510 023737 001126 001124 ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
(1) 021516 001401 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 10KHZ PULSE GENERATED?  
(1) BEQ 4$ ;/NO - GO TO NEXT CHECK.  
(2)
```

:::*****>> ERROR <<*****

```
(1) 021520 104015 ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE  
(1) ;/GENERATED A SECOND 10KHZ PULSE  
(1) ;/ON ONLY 9 100KHZ PULSES.  
(2)
```

:::*****>> ERROR <<*****

```
(1) 021522 4$:  
3364  
(5) :*****  
(4) :*TEST 145 *TEST CLOCK B'S 1KHZ DIVIDER  
(5) :*  
(5) :+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ  
(5) :+BY 10 TO GIVE US A 100HZ CLK L PULSE.  
(5) :+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND  
(5) :+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ  
(5) :+PULSES.  
(5) :+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
```

```

(5)
(5)
(6)
(6)
(6)
(4)
(3) 021522 000004
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 021524 005037 001354
(2)
(2)
(2)
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(2)
(1) 021560 012737 004040 001354
(2)
(2)
(2)
(2)
(1) 021606 052737 000010 001354
(2)
(2)
(1) 021624 005237 001354
(2)
(2)
(1) 021640 012700 176030
(1)
(1) 021644
(1)
(2)
(2)
(1) 021654 052737 004000 001354
(2)
(2)
(2)
(1) 021702 005737 001126
(1) 021706 001002
(1)
(1)
(1)
(1)
(1)
(1) 021710 005200
(1) 021712 001354
(1)
(1) 021714 012737 000001 001124 10$:
(1)

```

```

;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
;*
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
*****
TST145: SCOPE

;/CLEAR CLOCK B.
;/CLEAR CLOCK A.

;/CLEAR B'S BUFFER + COUNT REGS.
;/DISABLE THE 1MHZ OSC.
;/RATE: 1KHZ
;/ENABLE CLOCK B.

CLR $TMDAT

;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
MOV #BIT11!BITS,$TMDAT

;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR

;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
BIS #10,$TMDAT

;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
INC $TMDAT

;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
MOV #-1000.,R0 ;/SET TO GENERATE 1000. 1MHZ PULSES

1$: ;/GENERATE 1 1MHZ PULSE
;/HAS THE COUNTER ADVANCED?

;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT

;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR

;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/EXIT LOOP IF SO.
;/NOTE: WHEN WE DISABLED THE 1 MHZ.
;/ OSC., THE DIVIDER COULD HAVE
;/ HAD ANY COUNT IN IT.
;/AFTER THIS LOOP, WE SHOULD BE SUNK.

;/DONE 1000. 1MHZ PULSES?
;/IF NOT - DO ANOTHER.

MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.

```



```

(6)
(6)
(4)
(3) 022026 000004
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1) 022030 005037 001354 CLR $TMDAT ;/CLEAR CLOCK B.
(2) ;/CLEAR CLOCK A.
(2)
(2) ;/CLEAR B'S BUFFER + COUNT REGS.
(2) ;/DISABLE THE 1MHZ OSC.
(2) ;/RATE: 100HZ
(2) ;/ENABLE CLOCK B.
(2)
(2)
(2)
(2)
(2)
(1) 022064 012737 004040 001354
(2)
(2)
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(1) 022112 052737 000012 001354
(2)
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(2)
(1) 022130 005237 001354
(2)
(2)
(1) 022144 012700 154360
(1)
(1) 022150
(1)
(1)
(2)
(2)
(1) 022160 052737 004000 001354
(2)
(2)
(2)
(1) 022206 005737 001126
(1) 022212 001002
(1)
(1)
(1)
(1)
(1)
(1) 022214 005200 INC R0 ;/DONE 10000. 1MHZ PULSES?
(1) 022216 001354 BNE 1$ ;/IF NOT - DO ANOTHER.
(1)
(1) 022220 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
(1) ;/READ THE COUNTER
(2)
(2) ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.

```

```

;* PROBABLE SYNC POINT FOR THIS TEST:: 'LD BUFF A'
;*****
TST146: SCOPE

```

```

;/CLEAR CLOCK B.
;/CLEAR CLOCK A.
;/CLEAR B'S BUFFER + COUNT REGS.
;/DISABLE THE 1MHZ OSC.
;/RATE: 100HZ
;/ENABLE CLOCK B.

```

```

;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
MOV #BIT11!BITS,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
BIS #12,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
INC $TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
MOV #-10000.,R0 ;/SET TO GENERATE 10000. 1MHZ PULSES
1$: ;/GENERATE 1 1MHZ PULSE
;/HAS THE COUNTER ADVANCED?
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 10$ ;/EXIT LOOP IF SO.
;/NOTE: WHEN WE DISABLED THE 1 MHZ.
;/ OSC., THE DIVIDER COULD HAVE
;/ HAD ANY COUNT IN IT.
;/AFTER THIS LOOP, WE SHOULD BE SUNK.

```

```
(1)
(1) 022236 023737 001126 001124      CMP    $BDDAT,$GDDAT    ;/DID THE COUNTER ADVANCE ONCE?
(1) 022244 001402                      BEQ    2$                ;/IF YES - NEXT CHECK
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022246 104015                      ERROR   15                ;/ERROR - CLOCK B - 100HZ - PULSE
(1)                                     ;/NOT GENERATED WHEN 10 1KHZ PULSE
(1)                                     ;/WERE GENERATED.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022250 000430                      BR     4$
(1)
(1) 022252 012700 154361                2$:   MOV    #-9999.,RO    ;/GET THE NUMBER OF '1 MHZ' H PULSES
(1)                                     ;/NEED TO GIVE 9 1KHZ PULSES
(1) 022256                               3$:
(2)
(2)                                     ;*   MOV    @ASR,$TMDAT    ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
(1) 022266 052737 004000 001354        BIS    #BIT11,$TMDAT
(2)
(2)                                     ;*   MOV    $TMDAT,@ASR    ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(1) 022304 005200                       INC    RO                ;/IN ORDER TO CHECK TO SEE THAT
(1) 022306 001363                       BNE    3$                ;/WE DON'T GENERATE ANOTHER 100HZ PULSE
(1)
(2)
(2)                                     ;*   MOV    @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
(1) 022320 023737 001126 001124        CMP    $BDDAT,$GDDAT    ;/WAS ANOTHER 100HZ PULSE GENERATED?
(1) 022326 001401                       BEQ    4$                ;/NO - GO TO NEXT CHECK.
(1)
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022330 104015                      ERROR   15                ;/ERROR CLOCK B WE SEEM TO HAVE
(1)                                     ;/GENERATED A SECOND 100HZ PULSE
(1)                                     ;/ON ONLY 9 1KHZ PULSES.
(2)
      ::: $$$$$$$$$$$$$$$$$$$$$$$$$$$$>> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$
(1) 022332                               4$:
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(1)
(2)
(1)                                     .SBTTL
(1)                                     .SBTTL  END OF PASS ROUTINE
(1)                                     :::*****
(1)                                     ;*INCREMENT THE PASS NUMBER ($PASS)
(1)                                     ;*TYPE 'END PASS #XXXXX' (WHERE XXXXX IS A DECIMAL NUMBER)
(1)                                     ;*IF THERES A MONITOR GO TO IT
(1)                                     ;*IF THERE ISN'T JUMP TO LOOP
(1)
(1) 022332                               SEOP:
(2) 022332 000240                       NOP
(1) 022334 005037 001102                 CLR    $STNM            ;:ZERO THE TEST NUMBER
(1) 022340 005237 001206                 INC    $PASS            ;:INCREMENT THE PASS NUMBER
```

(1) 022344 042737 100000 001206
 (1) 022352 005327
 (1) 022354 000001
 (1) 022356 003022
 (1) 022360 012737
 (1) 022362 000001
 (1) 022364 022354
 (1) 022366 104401 022433
 (2) 022372 013746 001206
 (2) 022376 104405
 (1) 022400 104401 022430
 (1) 022404 013700 000042
 (1) 022410 001405
 (1) 022412 000005
 (1) 022414 004710
 (1) 022416 000240
 (1) 022420 000240
 (1) 022422 000240
 (1) 022424
 (1) 022424 000137
 (1) 022426 002334
 (1) 022430 377 377 000
 (1) 022433 015 042412 042116
 (1) 022440 050040 051501 020123
 (1) 022446 000043

BIC #100000,\$PASS ;;DON'T ALLOW A NEG. NUMBER
 DEC (PC)+ ;;LOOP?
 \$EOPCT: .WORD 1
 BGT \$DOAGN ;;YES
 MOV (PC)+,@(PC)+ ;;RESTORE COUNTER
 \$ENDCT: .WORD 1
 \$EOPCT
 TYPE \$SENDMG ;;TYPE 'END PASS #'
 MOV \$PASS,-(SP) ;;SAVE \$PASS FOR TYPEOUT
 TYPDS ;;GO TYPE--DECIMAL ASCII WITH SIGN
 TYPE \$ENULL ;;TYPE A NULL CHARACTER
 \$GET42: MOV @#42,R0 ;;GET MONITOR ADDRESS
 BEQ \$DOAGN ;;BRANCH IF NO MONITOR
 RESET ;;CLEAR THE WORLD
 \$ENDAD: JSR PC,(R0) ;;GO TO MONITOR
 NOP ;;SAVE ROOM
 NOP ;;FOR
 NOP ;;ACT11
 \$DOAGN:
 JMP @(PC)+ ;;RETURN
 \$RTNAD: .WORD LOOP
 \$ENULL: .BYTE -1,-1,0 ;;NULL CHARACTER STRING
 \$SENDMG: .ASCIZ <15><12>/END PASS #/

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.SBTTL *
 .SBTTL * SPECIAL I/O SIGNAL TESTS
 .SBTTL *
 .SBTTL * "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS
 :*
 :* THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
 :* PROVIDING SCOPE LOOP CAPABILITIES FOR "STP2 OUT" L
 :* AND "SCHMITT TRIG 1" IN.
 :*
 :* WHEN YOU LOAD AND START AT LOCATION 210, PROGRAM
 :* CONTROL IS TRANSFERRED HERE. "STP2 OUT" L PULSES ARE
 :* GENERATED BY 'LO STAT A HI' H + 'BD10' H (MAIN. STP2).
 :* PIN V ('STP2 OUT') IS WIRED TO PIN LL (SCHMITT TRIG1) FOR
 :* THIS TEST. "STP2 OUT" PULSES ARE RECEIVED AS "SCHMITT TRIG 1"
 :* PULSES WHICH SET CLOCK A'S STATUS REGISTER BIT 15.
 :* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
 :* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
 :* AN '*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
 :* TEST. SW13=1 WILL INHIBIT THIS FEATURE.
 :*
 :* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
 :*
 :* YOU MUST WIRE PINS V AND LL OF J1 TOGETHER AND INSTALL JUMPER W3
 :*
 :* LOGIC TEST (L + S 200) SHOULD BE RUN FIRST.
 :*


```
3457 022450 005037 001664 LS210: CLR .DVLS
3458 (1) 022454 005037 001104 1$: CLR $ICNT ;/CLEAR ITERATION COUNT
(1) 022460 012737 177704 001206 MOV #-60.,$PASS ;/SET PASS COUNT.
(1) ;/NOTE: PASS COUNT USED ONLY
(1) ;/ TO DETECT 60 PASSES SO
(1) ;/ IT CAN GENERATE A CRLF.
(1) ;/ AFTER CRLF IT WILL BE ZEROED.
(1) 022466 2$: CLR $TMDAT ;/CLEAR CLOCK A.
(1) 022466 005037 001354 ;/CLEAR CLOCK B.
(2) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
(2) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
(1)
3459 ;GENERATE AN 'STP2 OUT' PULSE
3460 ;AT THIS POINT YOU SHOULD
3461 ;SEE AN OUTPUT AT PIN V.
3462 ;PIN V SHOULD BE WIRED TO
3463 ;PIN LL FOR 'SCHMITT TRIG 1' IN.
3464
3465
3466 (1) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3467 (1) ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
3468 022532 052737 002000 001354 BIS #BIT10,$TMDAT ;GENERATE STP2
3469 (1) ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
3470 022550 000240 NOP
3471 022552 000240 NOP
3472 (1) ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
3473 022564 032737 100000 001354 BIT #BIT15,$TMDAT ;IS ST1 FLAG SET <BIT 15>
3474 022572 001001 BNE 3$ ;BR IF YES TO 3$:
3475
3476 ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

3477
3478 022574 104000 ERROR ;ERROR 'SCHMITT TRIG 1' IN NOT
3479 ;RECEIVED. HAVE YOU WIRED IT RIGHT?
3480 ;:; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

3481 022576 3$:
3482 (1) 022576 032777 020000 156334 BIT #BIT13,@SWR ;/INHIBIT '*' TYPEOUT?
(1) 022604 001330 BNE 2$ ;/YES - IGNORE ANY UPDATES.
(1)
(1) 022606 005237 001104 INC $ICNT ;/UPDATE COUNT.
(1) 022612 001325 BNE 2$ ;/IF NOT DONE 65,32' TIMES,
(1) ;/DO IT AGAIN.
(2) 022614 104401 022622 TYPE .65$ ;:TYPE ASCII STRING
```

(2) 022620 000401
(2) 022624
(1) 022624 005237 001206
(1) 022630 100716
(2) 022632 104401 022640
(2) 022636 000402
(2) 022644
(1) 022644 000703
(1)

BR 64\$;:GET OVER THE ASCIZ
65\$: .ASCIZ ##
64\$:
INC \$PASS ;/DONE 60 PASSES?
BMI 2\$;/NO - NO NEED FOR CR,LF.
TYPE ,67\$;:TYPE ASCIZ STRING
BR 66\$;:GET OVER THE ASCIZ
67\$: .ASCIZ <15><12>##
66\$:
BR 1\$

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3501
3502

.SBTTL ;* "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS
;*
;* THIS IS A SPECIAL TEST SECTION DEVOTED FOR TESTING AND
;* PROVIDING SCOPE LOOP CAPABILITIES FOR "STP1 OUT" AND
;* "SCHMITT TRIG2" IN.
;*
;* WHEN YOU LOAD AND START AT LOCATION 214, PROGRAM
;* CONTROL IS TRANSFERRED HERE. "STP1 OUT" L PULSES ARE
;* GENERATED BY 'LD STAT A HI' + 'BD12' H (MAIN ST1).
;* PIN DD ("STP1 OUT") IS WIRED TO PIN BB ("SCHMITT
;* TRIG 2") FOR THIS TEST. "STP1 OUT" PULSES ARE RECEIVED AS
;* "SCHMITT TRIG 2" PULSES WHICH WILL CLEAR CLOCK A'S
;* COUNT REGISTER IF MODE 3 IS SELECTED.
;* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
;* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
;* AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH
;* THE TEST. SW13=1 WILL INHIBIT THIS FEATURE.
;*
;* PROBABLE SYNC POINT FOR THIS TEST: 'LD STAT B'
;*
;* YOU MUST WIRE PINS DD AND BB OF J1 TOGETHER AND INSTALL JUMPER W4.
;*
;* LOGIC TESTS (L + S AT 200) SHOULD BE RUN FIRST.
;*

(1)
(1)
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3504
3505
3506
3507
3508 022646 005037 001664
3509
(1) 022652 005037 001104
(1) 022656 012737 177704 001206
(1)
(1)
(1)
(1)
(1)
(1) 022664
(1) 022664 005037 001354
(2)
(2)
(2)
(2)
(1)
3510

LS214: CLR .DVLS
1\$: CLR \$ICNT ;/CLEAR ITERATION COUNT
MOV #-60.,\$PASS ;/SET PASS COUNT.
;/NOTE: PASS COUNT USED ONLY
;/ TO DETECT 60 PASSES SO
;/ IT CAN GENERATE A CRLF.
;/ AFTER CRLF IT WILL BE ZEROED.
2\$: ;/CLEAR CLOCK A.
;/CLEAR CLOCK B.
;* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR
;* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR
;LOAD ALL ONES TO CLK A'S BUFFER + COUNT REG.

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 3563 023062 005037 001664
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 (1) 023066 005037 001104
 (1) 023072 012737 177704 001206
 (1)
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 (1) 023100
 (1) 023100 005037 001354
 (2)
 (2)
 (2)
 (2)
 (1)
 3565 023124 005037 001354
 3566
 3567
 (1)
 3568 023140 052737 011000 001354
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 (1)
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```
.SBTTL * 'SCHMITT TRIG 3' IN, 'ST3 OUT' TESTS
:*
:* THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
:* PROVIDING SCOPE LOOP CAPABILITIES FOR 'SCHMITT TRIG 3'
:* AND 'ST3 OUT'.
:*
:* WHEN YOU LOAD AND START AT LOCATION 220, PROGRAM
:* CONTROL IS TRANSFERRED HERE. 'STP1' PULSES ARE GENERATED
:* BY 'LD STAT A H,' + 'BD12' H (MAIN STP1). PIN DD ('STP1 OUT')
:* IS WIRED TO PIN T ('SCHMITT TRIG 3'), 'SCHMITT TRIG 3' PULSES
:* GIVE US 'ST3 OUT' PULSES. PIN L ('ST3 OUT') IS WIRED
:* TO PIN BB ('SCHMITT TRIG2'), AND 'SCHMITT TRIG 2' WILL SET
:* CLOCK A'S STATUS REGISTER BIT 7.
:* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
:* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
:* AN '*' IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
:* TEST. SW13=1 WILL INHIBIT THIS FEATURE.
:*
:* PROBABLE SYNC POINT FOR THIS TEST:: 'LD STAT B'
:*
:* YOU MUST WIRE PINS DD TO T OF J1 TOGETHER, AS WELL AS
:* PINS L TO BB OF J1 TOGETHER AND INSTALL JUMPERS W4 AND W5.
:*
:* TESTS LS210 AND LS214 SHOULD BE RUN FIRST.
:*
LS220: CLR .DVLS
1$: CLR $ICNT ;/CLEAR ITERATION COUNT
MOV #-60.,$PASS ;/SET PASS COUNT.
;/NOTE: PASS COUNT USED ONLY
;/ TO DETECT 60 PASSES SO
;/ IT CAN GENERATE A CRLF.
;/ AFTER CRLF IT WILL BE ZEROED.
;/CLEAR CLOCK A.
;/CLEAR CLOCK B.
2$: CLR $TMDAT
:* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
:* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;GENERATE A 'STP2 OUT' PULSE.
CLR $TMDAT
:* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT12!BIT9,$TMDAT
:* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;AT THIS POINT YOU SHOULD SEE AN
;OUTPUT AT PIN DD. PIN DD SHOULD BE
;WIRED TO PIN T TO GIVE 'SCHMITT TRIG3'
;INPUT WHICH IN TURN SHOULD GIVE
;AN OUTPUT AT PIN L ('ST3'). PIN
;L BEING WIRED TO PIN BB ('SCHMITT
```


3640 023404
3641
(1) 023404 032777 020000 155526
(1) 023412 001324
(1)
(1) 023414 005237 001104
(1) 023420 001321
(1)
(1)
(2) 023422 104401 023430
(2) 023426 000401
(2)
(2) 023432
(1)
(1) 023432 005237 001206
(1) 023436 100712
(2) 023440 104401 023446
(2) 023444 000402
(2)
(2) 023452
(1) 023452 000677
(1)

4\$:
BIT #BIT13,@SWR ;/INHIBIT "*" TYPEOUT?
BNE 2\$;/YES - IGNORE ANY UPDATES.

INC \$ICNT ;/UPDATE COUNT.
BNE 2\$;/IF NOT DONE 65,324 TIMES.
;/DO IT AGAIN.

TYPE ,65\$;:TYPE ASCIZ STRING
BR ,64\$;:GET OVER THE ASCIZ
::65\$: .ASCIZ ##
64\$:

INC \$PASS ;/DONE 60 PASSES?
BMI 2\$;/NO - NO NEED FOR CR,LF.
TYPE ,67\$;:TYPE ASCIZ STRING
BR ,66\$;:GET OVER THE ASCIZ
::67\$: .ASCIZ <15><12>##
66\$:
BR 1\$

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(1)
(1)
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(1)
(1)
(1)
(1)
(1)
(1)

.SBTTL * "B EVENT OUT" TEST
*
*THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
*PROVIDING SCOPE LOOP CAPABILITIES FOR "B EVENT OUT".
*
*WHEN YOU LOAD AND START AT LOCATION 230, PROGRAM
*CONTROL IS TRANSFERRED HERE. "B EVENT OUT" PULSES ARE
*GENERATED BY CLOCK B OVERFLOWS. PIN TT
*("B EVENT OUT") IS WIRED TO PIN BB ("SCHMITT TRIG 2")
*"SCHMITT TRIG 2" PULSES WILL SET CLOCK A'S CSR BIT 7.
*IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIQ.
*AND ERROR SWITCH REGISTER OPTIONS ARE USED.
AN "" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE TEST.
*SW13=1 WILL INHIBIT THIS FEATURE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"
*
*YOU MUST WIRE PINS TT AND BB OF J1 TOGETHER AND INSTALL JUMPER W4.
*
*TEST LS210 SHOULD BE RUN FIRST.
*
LS230: CLR .DVLS
1\$: CLR \$ICNT ;/CLEAR ITERATION COUNT
MOV #-60.,\$PASS ;/SET PASS COUNT.
;/NOTE: PASS COUNT USED ONLY
;/ TO DETECT 60 PASSES SO
;/ IT CAN GENERATE A CRLF.
;/ AFTER CRLF IT WILL BE ZEROED.
;/CLEAR CLOCK A.


```
(2) 023652 000401 BR 64$ ;;GET OVER THE ASCIZ
(2) ;;65$: .ASCIZ #*#
(2) 023656 64$:
(1)
(1) 023656 005237 001206 INC $PASS ;/DONE 60 PASSES?
(1) 023662 100703 BMI 2$ ;/NO - NO NEED FOR CR,LF.
(2) 023664 104401 023672 TYPE ,67$ ;;TYPE ASCIZ STRING
(2) 023670 000402 BR 66$ ;;GET OVER THE ASCIZ
(2) ;;67$: .ASCIZ <15><12>##
(2) 023676 66$:
(1) 023676 000670 BR 1$
(1)
3697
3698 ;*ROUTINE TO HANDLE TRAPS TO LOC 4, 10 AND .
3699 ;*INTERRUPTS TO WRONG VECTORS.
3700 ;*.+2, IOTT(TRAPS) WERE PUT IN LOCATIONS 4-1000
3701
3702
3703 IOTRD:
3704 023700 011637 024050 024050 MOV (R6),2$ ;GET WHERE WE TRAPPED TO.
3705 023704 162737 000004 SUB #4,2$ ;=WHERE R6 RETURN 10-4
3706 023712 104401 023720 TYPE ,65$ ;;TYPE ASCIZ STRING
(1) 023716 000412 BR 64$ ;;GET OVER THE ASCIZ
(1) ;;65$: .ASCIZ <15><12>#ILLEGAL TRAP TO: #
(1) 64$:
3707 023744
3708 023744 013746 024050 MOV 2$,-(SP) ;;SAVE 2$ FOR TYPEOUT
(1) 023750 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
3709
3710 023752 104401 023760 TYPE ,67$ ;;TYPE ASCIZ STRING
(1) 023756 000407 BR 66$ ;;GET OVER THE ASCIZ
(1) ;;67$: .ASCIZ # FROM LOC.: #
(1) 66$:
3711 023776
3712 023776 062706 000004 ADD #4,R6 ;POINT TO WHERE WE TRAPPED FROM.
3713
3714 024002 011637 024052 MOV (R6),3$ ;PICK UP LOC
3715 024006 162737 000002 024052 SUB #2,3$ ;FROM REAL ADDR.
3716 024014 013746 024052 MOV 3$,-(SP) ;;SAVE 3$ FOR TYPEOUT
(1) 024020 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
3717
3718 024022 023727 024050 000004 CMP 2$,#4 ;DID WE TRAP TO LOC 4?
3719 024030 001405 BEQ 1$ ;IF SO - DON'T RETURN!
3720 024032 023727 024050 000010 CMP 2$,#10 ;DID WE TRAP TO LOC. 10?
3721 024040 001401 BEQ 1$ ;IF SO - DON'T RETURN!
3722 024042 000002 RTI ;TRY RETURNING.
3723
3724
3725 024044 000000 1$: HALT ;WE STOPPED HERE BECAUSE WE TRAPPED
3726 024046 000776 BR 1$ ;TO LOC 4 OR LOC 10. THIS IS A
3727 ;FATAL CONDITION THAT WE CAN NOT
3728 ;RECOVER FROM.
3729
3730
```


(1)	024172	010503					MOV	R5,R3	
(1)	024174	006103			3\$:		ROL	R3	::GET LSB OF THIS DIGIT
(1)	024176	105337	024300				DECB	\$OMODE	::TYPE THIS DIGIT?
(1)	024202	100016					BPL	7\$::BR IF NO
(1)	024204	042703	177770				BIC	#177770,R3	::GET RID OF JUNK
(1)	024210	001002					BNE	4\$::TEST FOR 0
(1)	024212	005704					TST	R4	::SUPPRESS THIS 0?
(1)	024214	001403					BEQ	5\$::BR IF YES
(1)	024216	005204			4\$:		INC	R4	::DON'T SUPPRESS ANYMORE 0'S
(1)	024220	052703	000060				BIS	#'0,R3	::MAKE THIS DIGIT ASCII
(1)	024224	052703	000040			5\$:	BIS	#',R3	::MAKE ASCII IF NOT ALREADY
(1)	024230	110337	024274				MOVB	R3,8\$::SAVE FOR TYPING
(1)	024234	104401	024274				TYPE	,8\$::GO TYPE THIS DIGIT
(1)	024240	105337	024276			7\$:	DECB	\$OCNT	::COUNT BY 1
(1)	024244	003347					BGT	2\$::BR IF MORE TO DO
(1)	024246	002402					BLT	6\$::BR IF DONE
(1)	024250	005204					INC	R4	::INSURE LAST DIGIT ISN'T A BLANK
(1)	024252	000744					BR	2\$::GO DO THE LAST DIGIT
(1)	024254	012605			6\$:		MOV	(SP)+,R5	::RESTORE R5
(1)	024256	012604					MOV	(SP)+,R4	::RESTORE R4
(1)	024260	012603					MOV	(SP)+,R3	::RESTORE R3
(1)	024262	016666	000002	000004			MOV	2(SP),4(SP)	::SET THE STACK FOR RETURNING
(1)	024270	012616					MOV	(SP)+,(SP)	
(1)	024272	000002					RTI		::RETURN
(1)	024274	000			8\$:		.BYTE	0	::STORAGE FOR ASCII DIGIT
(1)	024275	000					.BYTE	0	::TERMINATOR FOR TYPE ROUTINE
(1)	024276	000					\$OCNT:	.BYTE 0	::OCTAL DIGIT COUNTER
(1)	024277	000					\$OFILL:	.BYTE 0	::ZERO FILL SWITCH
(1)	024300	000000					\$OMODE:	.WORD 0	::NUMBER OF DIGITS TO TYPE
3738							.SBTTL	ERROR HANDLER ROUTINE	
(1)	:*****								
(2)	:*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,								
(1)	:*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL								
(1)	:*AND GO TO \$ERRTYP ON ERROR								
(1)	:*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:								
(1)	:*SW15=1 HALT ON ERROR								
(1)	:*SW13=1 INHIBIT ERROR TYPEOUTS								
(1)	:*SW10=1 BELL ON ERROR								
(1)	:*SW09=1 LOOP ON ERROR								
(1)	:*CALL								
(1)	:* ERROR N ;:ERROR=EMT AND N=ERROR ITEM NUMBER								
(1)	\$ERROR:								
(1)	024302	104407			7\$:		CKSWR		::TEST FOR CHANGE IN SOFT-SWR
(1)	024304	105237	001103				INCB	\$ERFLG	::SET THE ERROR FLAG
(1)	024310	001775					BEQ	7\$::DON'T LET THE FLAG GO TO ZERO
(1)	024312	013777	001102	154622			MOV	\$STNM,@DISPLAY	::DISPLAY TEST NUMBER AND ERROR FLAG
(1)	024320	032777	002000	154612			BIT	#BIT10,@SWR	::BELL ON ERROR?
(1)	024326	001402					BEQ	1\$::NO - SKIP
(1)	024330	104401	001170				TYPE	\$BELL	::RING BELL
(1)	024334	005237	001112			1\$:	INC	\$ERTTL	::COUNT THE NUMBER OF ERRORS
(1)	024340	011637	001116				MOV	(SP),\$ERRPC	::GET ADDRESS OF ERROR INSTRUCTION
(1)	024344	162737	000002	001116			SUB	#2,\$ERRPC	
(1)	024352	117737	154540	001114			MOVB	@\$ERRPC,\$ITEMB	::STRIP AND SAVE THE ERROR ITEM CODE
(1)	024360	032777	020000	154552			BIT	#BIT13,@SWR	::SKIP TYPEOUT IF SET

(1) 024366 001004
(1) 024370 004737 024502
(1) 024374 104401 001175
(1) 024400
(1) 024400 122737 000001 001220
(1) 024406 001007
(1) 024410 113737 001114 024422
(1) 024416 004737 026432
(1) 024422 000
(1) 024423 000
(1) 024424 000777
(1) 024426 005777 154506
(1) 024432 100002
(1) 024434 000000
(1) 024436 104407
(1) 024440 032777 001000 154472
(1) 024446 001402
(1) 024450 013716 001110
(1) 024454 005737 001166
(1) 024460 001402
(1) 024462 013716 001166
(1) 024466
(1) 024466 022737 022414 000042
(1) 024474 001001
(1) 024476 000000
(1) 024500
(1) 024500 000002

BNE 20\$::SKIP TYPEOUTS
JSR PC,\$ERRTYP ::GO TO USER ERROR ROUTINE
TYPE , \$CRLF
20\$: CMPB #APTENV,\$ENV ::RUNNING IN APT MODE
BNE 2\$::NO,SKIP APT ERROR REPORT
MOVB \$ITEMB,21\$::SET ITEM NUMBER AS ERROR NUMBER
JSR PC,\$ATY4 ::REPORT FATAL ERROR TO APT
21\$: .BYTE 0
.BYTE 0
22\$: BR 22\$::APT ERROR LOOP
2\$: TST @SWR ::HALT ON ERROR
BPL 3\$::SKIP IF CONTINUE
HALT ::HALT ON ERROR!
CKSWR ::TEST FOR CHANGE IN SOFT-SWR
3\$: BIT #BIT09,@SWR ::LOOP ON ERROR SWITCH SET?
BEQ 4\$::BR IF NO
MOV \$LPERR,(SP) ::FUDGE RETURN FOR LOOPING
4\$: TST \$ESCAPE ::CHECK FOR AN ESCAPE ADDRESS
BEQ 5\$::BR IF NONE
MOV \$ESCAPE,(SP) ::FUDGE RETURN ADDRESS FOR ESCAPE
5\$: CMP #SENDAD,@#42 ::ACT-11 AUTO-ACCEPT?
BNE 6\$::BRANCH IF NO
HALT ::YES
6\$: RTI ::RETURN
.SBTTL ERROR MESSAGE TYPEOUT ROUTINE

3739

(1)
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(1)
(1) 024502
(1) 024502 104401 001175
(1) 024506 010046
(1) 024510 005000
(1) 024512 153700 001114
(1) 024516 001004
(1)
(2) 024520 013746 001116
(2)
(2) 024524 104402
(1) 024526 000426
(1) 024530 005300
(1) 024532 006300
(1) 024534 006300
(1) 024536 006300
(1) 024540 062700 001356
(1) 024544 012037 024554
(1) 024550 001404
(1) 024552 104401
(1) 024554 000000
(1) 024556 104401 001175
(1) 024562 012037 024572

*THIS ROUTINE USES THE "ITEM CONTROL BYTE" (\$ITEMB) TO DETERMINE WHICH
*ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE "ERROR TABLE" (\$ERRTB),
*AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

\$ERRTYP:
TYPE , \$CRLF ::'CARRIAGE RETURN' & 'LINE FEED'
MOV RO, -(SP) ::SAVE RO
CLR RO ::PICKUP THE ITEM INDEX
BISB @#\$ITEMB,RO
BNE 1\$::IF ITEM NUMBER IS ZERO, JUST
MOV \$ERRPC, -(SP) ::TYPE THE PC OF THE ERROR
::SAVE \$ERRPC FOR TYPEOUT
::ERROR ADDRESS
TYPYC ::GO TYPE--OCTAL ASCII(ALL DIGITS)
BR 6\$::GET OUT
1\$: DEC RO ::ADJUST THE INDEX SO THAT IT WILL
ASL RO :: WORK FOR THE ERROR TABLE
ASL RO
ASL RO
ADD # \$ERRTB,RO ::FORM TABLE POINTER
MOV (RO)+,2\$::PICKUP "ERROR MESSAGE" POINTER
BEQ 3\$::SKIP TYPEOUT IF NO POINTER
TYPE ::TYPE THE "ERROR MESSAGE"
2\$: .WORD 0 ::"ERROR MESSAGE" POINTER GOES HERE
TYPE , \$CRLF ::'CARRIAGE RETURN' & 'LINE FEED'
3\$: MOV (RO)+,4\$::PICKUP "DATA HEADER" POINTER

```

(1) 024566 001404          BEQ      5$          ;;SKIP TYPEOUT IF 0
(1) 024570 104401          TYPE          ;;TYPE THE 'DATA HEADER'
(1) 024572 000000          4$: .WORD      0          ;;'DATA HEADER' POINTER GOES HERE
(1) 024574 104401 001175  TYPE      ,%CRLF        ;;'CARRIAGE RETURN' & 'LINE FEED'
(1) 024600 011000          5$: MOV      (R0),R0      ;;PICKUP 'DATA TABLE' POINTER
(1) 024602 001004          BNE      7$          ;;GO TYPE THE DATA
(1) 024604 012600          6$: MOV      (SP)+,R0     ;;RESTORE R0
(1) 024606 104401 001175  TYPE      ,%CRLF        ;;'CARRIAGE RETURN' & 'LINE FEED'
(1) 024612 000207          RTS      PC          ;;RETURN
(1) 024614          7$:          ;;
(2) 024614 013046          MOV      @ (R0)+,-(SP)  ;;SAVE @ (R0)+ FOR TYPEOUT
(2) 024616 104402          TYPDC          ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
(1) 024620 005710          TST      (R0)         ;;IS THERE ANOTHER NUMBER?
(1) 024622 001770          BEQ      6$          ;;BR IF NO
(1) 024624 104401 024632  TYPE      ,8$          ;;TYPE TWO(2) SPACES
(1) 024630 000771          BR      7$          ;;LOOP
(1) 024632 020040 000      8$: .ASCIZ  / /          ;;TWO(2) SPACES
(1) 024636 024636          .EVEN
3740 .SBTTL  CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
(1)          ;;*****
(2)          ;;*THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 5-DIGIT
(1)          ;;*SIGNED DECIMAL (ASCII) NUMBER AND TYPE IT. DEPENDING ON WHETHER THE
(1)          ;;*NUMBER IS POSITIVE OR NEGATIVE A SPACE OR A MINUS SIGN WILL BE TYPED
(1)          ;;*BEFORE THE FIRST DIGIT OF THE NUMBER. LEADING ZEROS WILL ALWAYS BE
(1)          ;;*REPLACED WITH SPACES.
(1)          ;;*CALL:
(1)          ;;*
(1)          MOV      NUM,-(SP)          ;;PUT THE BINARY NUMBER ON THE STACK
(1)          TYPDS          ;;GO TO THE ROUTINE
(1)          ;;*
(1)          $TYPDS:
(3) 024636 010046          MOV      R0,-(SP)     ;;PUSH R0 ON STACK
(3) 024640 010146          MOV      R1,-(SP)     ;;PUSH R1 ON STACK
(3) 024642 010246          MOV      R2,-(SP)     ;;PUSH R2 ON STACK
(3) 024644 010346          MOV      R3,-(SP)     ;;PUSH R3 ON STACK
(3) 024646 010546          MOV      R5,-(SP)     ;;PUSH R5 ON STACK
(1) 024650 012746 020200  MOV      #20200,-(SP)  ;;SET BLANK SWITCH AND SIGN
(1) 024654 016605 000020  MOV      20(SP),R5    ;;GET THE INPUT NUMBER
(1) 024660 100004          BPL      1$          ;;BR IF INPUT IS POS.
(1) 024662 005405          NEG      R5          ;;MAKE THE BINARY NUMBER POS.
(1) 024664 112766 000055 000001  MOVB     #'-',1(SP)   ;;MAKE THE ASCII NUMBER NEG.
(1) 024672 005000          1$: CLR      R0          ;;ZERO THE CONSTANTS INDEX
(1) 024674 012703 025052  MOV      #5DBLK,R3    ;;SETUP THE OUTPUT POINTER
(1) 024700 112723 000040  MOVB     #'',(R3)+    ;;SET THE FIRST CHARACTER TO A BLANK
(1) 024704 005002          2$: CLR      R2          ;;CLEAR THE BCD NUMBER
(1) 024706 016001 025042  MOV      $DTBL(R0),R1 ;;GET THE CONSTANT
(1) 024712 160105          3$: SUB      R1,R5     ;;FORM THIS BCD DIGIT
(1) 024714 002402          BLT      4$          ;;BR IF DONE
(1) 024716 005202          INC      R2          ;;INCREASE THE BCD DIGIT BY 1
(1) 024720 000774          BR      3$
(1) 024722 060105          4$: ADD      R1,R5     ;;ADD BACK THE CONSTANT
(1) 024724 005702          TST      R2          ;;CHECK IF BCD DIGIT=0
(1) 024726 001002          BNE      5$          ;;FALL THROUGH IF 0
(1) 024730 105716          TSTB    (SP)         ;;STILL DOING LEADING 0'S?
(1) 024732 100407          BMI      7$          ;;BR IF YES
(1) 024734 106316          5$: ASLB     (SP)     ;;MSD?

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(1) 025130 000417 BR 7$ ;:LOOP ON THE PRESENT TEST
(1) 025132 6$:;#####END OF CODE FOR THE XOR TESTER#####
(1) 025132 032777 000400 154000 BIT #BIT08,@SWR ;:LOOP ON SPEC. TEST?
(1) 025140 001404 BEQ 2$ ;:BR IF NO
(1) 025142 127737 153772 001102 CMPB @SWR,$STNM ;:ON THE RIGHT TEST? SWR<7:0>
(1) 025150 001433 BEQ $OVER ;:BR IF YES
(1) 025152 105737 001103 2$: TSTB $ERFLG ;:HAS AN ERROR OCCURRED?
(1) 025156 001412 BEQ $SVLAD ;:BR IF NO
(1) 025160 032777 001000 153752 BIT #BIT09,@SWR ;:LOOP ON ERROR?
(1) 025166 001404 BEQ 4$ ;:BR IF NO
(1) 025170 013737 001110 001106 7$: MOV $LPERR,$LPADR ;:SET LOOP ADDRESS TO LAST SCOPE
(1) 025176 000420 BR $OVER
(1) 025200 105037 001103 4$: CLR $ERFLG ;:ZERO THE ERROR FLAG
(1) 025204 105237 001102 $SVLAD: INCB $STNM ;:COUNT TEST NUMBERS
(1) 025210 113737 001102 001204 MOV $STNM,$TESTN ;:SET TEST NUMBER IN APT MAILBOX
(1) 025216 011637 001106 MOV (SP),$LPADR ;:SAVE SCOPE LOOP ADDRESS
(1) 025222 011637 001110 MOV (SP),$LPERR ;:SAVE ERROR LOOP ADDRESS
(1) 025226 005037 001166 CLR $ESCAPE ;:CLEAR THE ESCAPE FROM ERROR ADDRESS
(1) 025232 112737 000001 001115 MOV #1,$ERMAX ;:ONLY ALLOW ONE(1) ERROR ON NEXT TEST
(1) 025240 013777 001102 153674 $OVER: MOV $STNM,@DISPLAY ;:DISPLAY TEST NUMBER
(1) 025246 013716 001106 MOV $LPADR,(SP) ;:FUDGE RETURN ADDRESS
(1) 025252 000002 RTI ;:FIXES PS

```

```

3742 .SBTTL READ AN OCTAL NUMBER FROM THE TTY
(1) ;:*****
(2) ;:*THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
(1) ;:*CHANGE IT TO BINARY.
(1) ;:*CALL:
(1) ;:* RDOCT ;:READ AN OCTAL NUMBER
(1) ;:* RETURN HERE ;:LOW ORDER BITS ARE ON TOP OF THE STACK
(1) ;:* ;:HIGH ORDER BITS ARE IN $HIOCT

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(1) 025254 011646 000004 000002 $RDOCT: MOV (SP),-(SP) ;:PROVIDE SPACE FOR THE
(1) 025256 016666 MOV 4(SP),2(SP) ;:INPUT NUMBER
(3) 025264 010046 MOV R0,-(SP) ;:PUSH R0 ON STACK
(3) 025266 010146 MOV R1,-(SP) ;:PUSH R1 ON STACK
(3) 025270 010246 MOV R2,-(SP) ;:PUSH R2 ON STACK
(1) 025272 104411 1$: RDLIN ;:READ AN ASCII LINE
(1) 025274 012600 MOV (SP)+,R0 ;:GET ADDRESS OF 1ST CHARACTER
(1) 025276 005001 CLR R1 ;:CLEAR DATA WORD
(1) 025300 005002 CLR R2
(1) 025302 112046 2$: MOV (R0)+,-(SP) ;:PICKUP THIS CHARACTER
(1) 025304 001412 BEQ 3$ ;:IF ZERO GET OUT
(1) 025306 006301 ASL R1 ;:*2
(1) 025310 006102 ROL R2
(1) 025312 006301 ASL R1 ;:*4
(1) 025314 006102 ROL R2
(1) 025316 006301 ASL R1 ;:*8
(1) 025320 006102 ROL R2
(1) 025322 042716 177770 BIC #^C7,(SP) ;:STRIP THE ASCII JUNK
(1) 025326 062601 ADD (SP)+,R1 ;:ADD IN THIS DIGIT
(1) 025330 000764 BR 2$ ;:LOOP
(1) 025332 005726 3$: TST (SP)+ ;:CLEAN TERMINATOR FROM STACK
(1) 025334 010166 MOV R1,12(SP) ;:SAVE THE RESULT
(1) 025340 010237 MOV R2,$HIOCT
(3) 025344 012602 MOV (SP)+,R2 ;:POP STACK INTO R2

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(3)	025346	012601			MOV	(SP)+,R1	::POP STACK INTO R1
(3)	025350	012600			MOV	(SP)+,R0	::POP STACK INTO R0
(1)	025352	000002			RTI		::RETURN
(1)	025354	000000			\$HI OCT: .WORD	0	::HIGH ORDER BITS GO HERE
3743					.SBTTL	TTY INPUT ROUTINE	
(1)							::*****
(2)					.ENABL	LSB	
(1)							::*****
(1)					*SOFTWARE SWITCH REGISTER CHANGE ROUTINE.		
(1)					*ROUTINE IS ENTERED FROM THE TRAP HANDLER, AND WILL		
(1)					*SERVICE THE TEST FOR CHANGE IN SOFTWARE SWITCH REGISTER TRAP CALL		
(1)					*WHEN OPERATING IN TTY FLAG MODE.		
(1)	025356	022737	000176	001140	\$CKSWR: CMP	#SWREG,SWR	::IS THE SOFT-SWR SELECTED?
(1)	025364	001074			BNE	15\$::BRANCH IF NO
(1)	025366	105777	153552		TSTB	@\$TKS	::CHAR THERE?
(1)	025372	100071			BPL	15\$::IF NO, DON'T WAIT AROUND
(1)	025374	117746	153546		MOVB	@\$TKB,-(SP)	::SAVE THE CHAR
(1)	025400	042716	177600		BIC	#^C177,(SP)	::STRIP-OFF THE ASCII
(1)	025404	022726	000007		CMP	#7,(SP)+	::IS IT A CONTROL G?
(1)	025410	001062			BNE	15\$::NO, RETURN TO USER
(1)	025412	123727	001134	000001	CMPB	\$AUTOB,#1	::ARE WE RUNNING IN AUTO-MODE?
(1)	025420	001456			BEQ	15\$::BRANCH IF YES
(1)							
(1)	025422	104401	026103		\$GTSWR: TYPE	,\$CNTLG	::ECHO THE CONTROL-G (^G)
(1)	025426	104401	026110		TYPE	,\$MSWR	::TYPE CURRENT CONTENTS
(2)	025432	013746	000176		MOV	SWREG,-(SP)	::SAVE SWREG FOR TYPEOUT
(2)	025436	104402			TYPOC		::GO TYPE--OCTAL ASCII(ALL DIGITS)
(1)	025440	104401	026121		TYPE	,\$MNEW	::PROMPT FOR NEW SWR
(1)	025444	005046			19\$: CLR	-(SP)	::CLEAR COUNTER
(1)	025446	005046			CLR	-(SP)	::THE NEW SWR
(1)	025450	105777	153470		7\$: TSTB	@\$TKS	::CHAR THERE?
(1)	025454	100375			BPL	7\$::IF NOT TRY AGAIN
(1)							
(1)	025456	117746	153464		MOVB	@\$TKB,-(SP)	::PICK UP CHAR
(1)	025462	042716	177600		BIC	#^C177,(SP)	::MAKE IT 7-BIT ASCII
(1)							
(1)							
(1)	025466	021627	000025		9\$: CMP	(SP),#25	::IS IT A CONTROL-U?
(1)	025472	001005			BNE	10\$::BRANCH IF NOT
(1)	025474	104401	026076		TYPE	,\$CNTLU	::YES, ECHO CONTROL-U (^U)
(1)	025500	062706	000006		20\$: ADD	#6,SP	::IGNORE PREVIOUS INPUT
(1)	025504	000757			BR	19\$::LET'S TRY IT AGAIN
(1)							
(1)							
(1)	025506	021627	000015		10\$: CMP	(SP),#15	::IS IT A <CR>?
(1)	025512	001022			BNE	16\$::BRANCH IF NO
(1)	025514	005766	000004		TST	4(SP)	::YES, IS IT THE FIRST CHAR?
(1)	025520	001403			BEQ	11\$::BRANCH IF YES
(1)	025522	016677	000002	153410	MOV	2(SP),@SWR	::SAVE NEW SWR
(1)	025530	062706	000006		11\$: ADD	#6,SP	::CLEAR UP STACK
(1)	025534	104401	001175		14\$: TYPE	,\$CRLF	::ECHO <CR> AND <LF>
(1)	025540	123727	001135	000001	CMPB	\$INTAG,#1	::RE-ENABLE TTY KBD INTERRUPTS?
(1)	025546	001003			BNE	15\$::BRANCH IF NOT

(1)	025550	012777	000100	153366		MOV	#100,@STKS	::RE-ENABLE TTY KBD INTERRUPTS
(1)	025556	000002			15\$:	RTI		::RETURN
(1)	025560	004737	026344		16\$:	JSR	PC,\$TYPEC	::ECHO CHAR
(1)	025564	021627	000060			CMP	(SP),#60	::CHAR < 0?
(1)	025570	002420				BLT	18\$::BRANCH IF YES
(1)	025572	021627	000067			CMP	(SP),#67	::CHAR > 7?
(1)	025576	003015				BGT	18\$::BRANCH IF YES
(1)	025600	042726	000060			BIC	#60,(SP)+	::STRIP-OFF ASCII
(1)	025604	005766	000002			TST	2(SP)	::IS THIS THE FIRST CHAR
(1)	025610	001403				BEQ	17\$::BRANCH IF YES
(1)	025612	006316				ASL	(SP)	::NO, SHIFT PRESENT
(1)	025614	006316				ASL	(SP)	:: CHAR OVER TO MAKE
(1)	025616	006316				ASL	(SP)	:: ROOM FOR NEW ONE.
(1)	025620	005266	000002		17\$:	INC	2(SP)	::KEEP COUNT OF CHAR
(1)	025624	056616	177776			BIS	-2(SP),(SP)	::SET IN NEW CHAR
(1)	025630	000707				BR	7\$::GET THE NEXT ONE
(1)	025632	104401	001174		18\$:	TYPE	, \$QUES	::TYPE ?<CR><LF>
(1)	025636	000720				BR	20\$::SIMULATE CONTROL-U
(1)						.DSABL	LSB	

```

*****
*THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY
*CALL:
*      RDCHR          ::INPUT A SINGLE CHARACTER FROM THE TTY
*      RETURN HERE    ::CHARACTER IS ON THE STACK
*                          ::WITH PARITY BIT STRIPPED OFF
:
(1) 025640 011646 000004 0C0002 $RDCHR: MOV (SP),-(SP) ::PUSH DOWN THE PC
(1) 025642 016666 000004 0C0002 MOV 4(SP),2(SP) ::SAVE THE PS
(1) 025650 105777 153270 1$ TSTB @STKS ::WAIT FOR
(1) 025654 100375 BPL 1$ ::A CHARACTER
(1) 025656 117766 153264 000004 MOVB @STKB,4(SP) ::READ THE TTY
(1) 025664 042766 177770 000004 BIC #^C<177>,4(SP) ::GET RID OF JUNK IF ANY
(1) 025672 026677 000023 CMP 4(SP),#23 ::IS IT A CONTROL-S?
(1) 025700 000003 BNE 3$ ::BRANCH IF NO
(1) 025702 1 2$ TSTB @STKS ::WAIT FOR A CHARACTER
(1) 025706 2$ BPL 2$ ::LOOP UNTIL ITS THERE
(1) 025710 MOVB @STKB,-(SP) ::GET CHARACTER
(1) 025714 BIC #^C177,(SP) ::MAKE IT 7-BIT ASCII
(1) 025720 000004 CMP (SP)+,#21 ::IS IT A CONTROL-Q?
(1) 025724 001366 BNE 2$ ::IF NOT DISCARD IT
(1) 025726 000750 BR 1$ ::YES, RESUME
(1) 025730 026627 000004 000140 3$ CMP 4(SP),#140 ::IS IT UPPER CASE?
(1) 025736 002407 BLT 4$ ::BRANCH IF YES
(1) 025740 026627 000004 000175 CMP 4(SP),#175 ::IS IT A SPECIAL CHAR?
(1) 025746 003003 BGT 4$ ::BRANCH IF YES
(1) 025750 042766 000040 000004 BIC #40,4(SP) ::MAKE IT UPPER CASE
(1) 025756 000002 4$ RTI ::GO BACK TO USER
*****
*THIS ROUTINE WILL INPUT A STRING FROM THE TTY
*CALL:
*      RDLIN          ::INPUT A STRING FROM THE TTY
*      RETURN HERE    ::ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
*                          ::TERMINATOR WILL BE A BYTE OF ALL 0'S

```

(1)
(1) 025760 010346
(1) 025762 012703 026066
(1) 025766 022703 026076
(1) 025772 101405
(1) 025774 104410
(1) 025776 112613
(1) 026000 122713 000177
(1) 026004 001003
(1) 026006 104401 001174
(1) 026012 000763
(1) 026014 111337 026064
(1) 026020 104401 026064
(1) 026024 122723 000015
(1) 026030 001356
(1) 026032 105063 177777
(1) 026036 104401 001176
(1) 026042 012603
(1) 026044 011646
(1) 026046 016666 000004 000002
(1) 026054 012766 026066 000004
(1) 026062 000002
(1) 026064 000
(1) 026065 000
(1) 026066 000010
(1) 026076 052536 005015 000
(1) 026103 136 006507 000012
(1) 026110 005015 053523 020122
(1) 026116 020075 000
(1) 026121 040 047040 053505
(1) 026126 036440 000040
3744

```
$RDLIN: MOV R3, -(SP) ;;SAVE R3
1$: MOV #STTYIN, R3 ;;GET ADDRESS
2$: CMP #STTYIN+8., R3 ;;BUFFER FULL?
BLOS 4$ ;;BR IF YES
RDCHR ;;GO READ ONE CHARACTER FROM THE TTY
MOVB (SP)+, (R3) ;;GET CHARACTER
10$: CMPB #177, (R3) ;;IS IT A RUBOUT
BNE 3$ ;;SKIP IF NOT
4$: TYPE , $QUES ;;TYPE A '?'
BR 1$ ;;CLEAR THE BUFFER AND LOOP
3$: MOVB (R3), 9$ ;;ECHO THE CHARACTER
TYPE , 9$
CMPB #15, (R3)+ ;;CHECK FOR RETURN
BNE 2$ ;;LOOP IF NOT RETURN
CLRB -1(R3) ;;CLEAR RETURN (THE 15)
TYPE , $LF ;;TYPE A LINE FEED
MOV (SP)+, R3 ;;RESTORE R3
MOV (SP), -(SP) ;;ADJUST THE STACK AND PUT ADDRESS OF THE
MOV 4(SP), 2(SP) ;; FIRST ASCII CHARACTER ON IT
MOV #STTYIN, 4(SP)
RTI ;;RETURN
9$: .BYTE 0 ;;STORAGE FOR ASCII CHAR. TO TYPE
.BYTE 0 ;;TERMINATOR
STTYIN: .BLKB 8. ;;RESERVE 8 BYTES FOR TTY INPUT
$CNTLU: .ASCIZ /^U/<15><12> ;;CONTROL 'U'
$CNTLG: .ASCIZ /^G/<15><12> ;;CONTROL 'G'
$MSWR: .ASCIZ <15><12>/SWR = /
$MNEW: .ASCIZ / NEW = /
.SBTTL TYPE ROUTINE
```

```
*****
*ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
*THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
*NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
*NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
*NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
*
*CALL:
*1) USING A TRAP INSTRUCTION
* TYPE ,MESADR ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
*OR
* TYPE
* MESADR
*
$TYPE: TSTB $TFPLG ;;IS THERE A TERMINAL?
BPL 1$ ;;BR IF YES
HALT ;;HALT HERE IF NO TERMINAL
BR 3$ ;;LEAVE
1$: MOV R0, -(SP) ;;SAVE R0
MOV @2(SP), R0 ;;GET ADDRESS OF ASCIZ STRING
CMPB #APTENV, $ENV ;;RUNNING IN APT MODE
BNE 62$ ;;NO, GO CHECK FOR APT CONSOLE
```

```

(1) 026162 132737 000100 001221      BITB  #APTSPOOL,$ENVM  ;;SPOOL MESSAGE TO APT
(1) 026170 001405                      BEQ   62$              ;;NO,GO CHECK FOR CONSOLE
(1) 026172 010037 026202              MOV   RO,61$          ;;SETUP MESSAGE ADDRESS FOR APT
(1) 026176 004737 026422              JSR   PC,$ATY3        ;;SPOOL MESSAGE TO APT
(1) 026202 000000                      .WORD 0               ;;MESSAGE ADDRESS
(1) 026204 132737 000040 001221      61$: BITB  #APTCSUP,$ENVM  ;;APT CONSOLE SUPPRESSED
(1) 026212 001003                      BNE   60$              ;;YES,SKIP TYPE OUT
(1) 026214 112046                      2$:  MOVB (RO)+,-(SP)  ;;PUSH CHARACTER TO BE TYPED ONTO STACK
(1) 026216 001005                      BNE   4$               ;;BR IF IT ISN'T THE TERMINATOR
(1) 026220 005726                      TST  (SP)+            ;;IF TERMINATOR POP IT OFF THE STACK
(1) 026222 012600                      60$: MOV   (SP)+,RO    ;;RESTORE RO
(1) 026224 062716 000002              3$:  ADD   #2,(SP)     ;;ADJUST RETURN PC
(1) 026230 000002                      RTI                      ;;RETURN
(1) 026232 122716 000011              4$:  CMPB  #HT,(SP)    ;;BRANCH IF <HT>
(1) 026236 001430                      BEQ   8$               ;;BRANCH IF NOT <CRLF>
(1) 026240 122716 000200              CMPB  #CRLF,(SP)
(1) 026244 001006                      BNE   5$               ;;POP <CR><LF> EQUIV
(1) 026246 005726                      TST  (SP)+            ;;TYPE A CR AND LF
(1) 026250 104401                      TYPE
(1) 026252 001175                      $CRLF
(1) 026254 105037 026410              CLRB  $CHARCNT        ;;CLEAR CHARACTER COUNT
(1) 026260 000755                      BR    2$               ;;GET NEXT CHARACTER
(1) 026262 004737 026344              5$:  JSR   PC,$TYPEC    ;;GO TYPE THIS CHARACTER
(1) 026266 123726 001156              6$:  CMPB  $FILLC,(SP)+ ;;IS IT TIME FOR FILLER CHARS.?
(1) 026272 001350                      BNE   2$               ;;IF NO GO GET NEXT CHAR.
(1) 026274 013746 001154              MOV   $NULL,-(SP)     ;;GET # OF FILLER CHARS. NEEDED
(1)                                ;;AND THE NULL CHAR.
(1) 026300 105366 000001              7$:  DECB  1(SP)       ;;DOES A NULL NEED TO BE TYPED?
(1) 026304 002770                      BLT  6$               ;;BR IF NO--GO POP THE NULL OFF OF STACK
(1) 026306 004737 026344              JSR   PC,$TYPEC       ;;GO TYPE A NULL
(1) 026312 105337 026410              DECB  $CHARCNT        ;;DO NOT COUNT AS A COUNT
(1) 026316 000770                      BR    7$              ;;LOOP
(1)
(1)                                ;HORIZONTAL TAB PROCESSOR
(1)
(1) 026320 112716 000040              8$:  MOVB  #' ,(SP)    ;;REPLACE TAB WITH SPACE
(1) 026324 004737 026344              9$:  JSR   PC,$TYPEC    ;;TYPE A SPACE
(1) 026330 132737 000007 026410      BITB  #7,$CHARCNT     ;;BRANCH IF NOT AT
(1) 026336 001372                      BNE   9$              ;;TAB STOP
(1) 026340 005726                      TST  (SP)+            ;;POP SPACE OFF STACK
(1) 026342 000724                      BR    2$              ;;GET NEXT CHARACTER
(1) 026344 105777 152600              $TYPEC: TSTB @ $TPS    ;;WAIT UNTIL PRINTER IS READY
(1) 026350 100375                      BPL  $TYPEC
(1) 026352 116677 000002 152572      MOVB  2(SP),@$TPB     ;;LOAD CHAR TO BE TYPED INTO DATA REG.
(1) 026360 122766 000015 000002      CMPB  #CR,2(SP)       ;;IS CHARACTER A CARRIAGE RETURN?
(1) 026366 001003                      BNE   1$              ;;BRANCH IF NO
(1) 026370 105037 026410              CLRB  $CHARCNT        ;;YES--CLEAR CHARACTER COUNT
(1) 026374 000406                      BR    $TYPEX          ;;EXIT
(1) 026376 122766 000012 000002      1$:  CMPB  #LF,2(SP)   ;;IS CHARACTER A LINE FEED?
(1) 026404 001402                      BEQ  $TYPEX           ;;BRANCH IF YES
(1) 026406 105227                      INCB  (PC)+           ;;COUNT THE CHARACTER
(1) 026410 000000                      $CHARCNT: .WORD 0    ;;CHARACTER COUNT STORAGE
(1) 026412 000207                      $TYPEX: RTS          PC
(1)
3745                                .SBTTL  APT COMMUNICATIONS ROUTINE
(1)

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```
(2)
(1) 026414 112737 000001 026660 $ATY1: MOVB #1,$FFLG ;;TO REPORT FATAL ERROR
(1) 026422 112737 000001 026656 SATY3: MOVB #1,$MFLG ;;TO TYPE A MESSAGE
(1) 026430 000403
(1) 026432 112737 000001 026660 SATY4: MOVB #1,$FFLG ;;TO ONLY REPORT FATAL ERROR
(1) 026440
(3) 026440 010046 MOV R0,-(SP) ;;PUSH R0 ON STACK
(3) 026442 010146 MOV R1,-(SP) ;;PUSH R1 ON STACK
(1) 026444 105737 026656 TSTB $MFLG ;;SHOULD TYPE A MESSAGE?
(1) 026450 001450 BEQ 5$ ;;IF NOT: BR
(1) 026452 122737 000001 001220 CMPB #APTENV,$ENV ;;OPERATING UNDER APT?
(1) 026460 001031 BNE 3$ ;;IF NOT: BR
(1) 026462 132737 000100 001221 BITB #APTPOOL,$ENVM ;;SHOULD SPOOL MESSAGES?
(1) 026470 001425 BEQ 3$ ;;IF NOT: BR
(1) 026472 017600 000004 MOV @4(SP),R0 ;;GET MESSAGE ADDR.
(1) 026476 062766 000002 000004 ADD #2,4(SP) ;;BUMP RETURN ADDR.
(1) 026504 005737 001200 1$: TST $MSGTYPE ;;SEE IF DONE W/ LAST XMISSION?
(1) 026510 001375 BNE 1$ ;;IF NOT: WAIT
(1) 026512 010037 001214 MOV R0,$MSGAD ;;PUT ADDR IN MAILBOX
(1) 026516 105720 2$: TSTB (R0)+ ;;FIND END OF MESSAGE
(1) 026520 001376 BNE 2$
(1) 026522 163700 001214 SUB $MSGAD,R0 ;;SUB START OF MESSAGE
(1) 026526 006200 ASR R0 ;;GET MESSAGE LENGTH IN WORDS
(1) 026530 010037 001216 MOV R0,$MSGGLT ;;PUT LENGTH IN MAILBOX
(1) 026534 012737 000004 001200 MOV #4,$MSGTYPE ;;TELL APT TO TAKE MSG.
(1) 026542 000413 BR 5$
(1) 026544 017637 000004 026570 3$: MOV @4(SP),4$ ;;PUT MSG ADDR IN JSR LINKAGE
(1) 026552 062766 000002 000004 ADD #2,4(SP) ;;BUMP RETURN ADDRESS
(3) 026560 013746 177776 MOV 177776,-(SP) ;;PUSH 177776 ON STACK
(1) 026564 004737 026132 JSR PC,$TYPE ;;CALL TYPE MACRO
(1) 026570 000000 4$: .WORD 0
(1) 026572 5$:
(1) 026572 105737 026660 10$: TSTB $FFLG ;;SHOULD REPORT FATAL ERROR?
(1) 026576 001416 BEQ 12$ ;;IF NOT: BR
(1) 026600 005737 001220 TST $ENV ;;RUNNING UNDER APT?
(1) 026604 001413 BEQ 12$ ;;IF NOT: BR
(1) 026606 005737 001200 11$: TST $MSGTYPE ;;FINISHED LAST MESSAGE?
(1) 026612 001375 BNE 11$ ;;IF NOT: WAIT
(1) 026614 017637 000004 001202 MOV @4(SP),$FATAL ;;GET ERROR #
(1) 026622 062766 000002 000004 ADD #2,4(SP) ;;BUMP RETURN ADDR.
(1) 026630 005237 001200 INC $MSGTYPE ;;TELL APT TO TAKE ERROR
(1) 026634 105037 026660 12$: CLRB $FFLG ;;CLEAR FATAL FLAG
(1) 026640 105037 026657 CLRB $LFLG ;;CLEAR LOG FLAG
(1) 026644 105037 026656 CLRB $MFLG ;;CLEAR MESSAGE FLAG
(3) 026650 012601 MOV (SP)+,R1 ;;POP STACK INTO R1
(3) 026652 012600 MOV (SP)+,R0 ;;POP STACK INTO R0
(1) 026654 000207 RTS PC ;;RETURN
(1) 026656 000 $MFLG: .BYTE 0 ;;MESSG. FLAG
(1) 026657 000 $LFLG: .BYTE 0 ;;LOG FLAG
(1) 026660 000 $FFLG: .BYTE 0 ;;FATAL FLAG
(1) 026662 .EVEN
(1) 000200 APTSIZE=200
(1) 000001 APTENV=001
(1) 000100 APTPOOL=100
(1) 000040 APTCSUP=040
3746 .SBTTL POWER DOWN AND UP ROUTINES
```

```

(1)
(2)
(1)
(1) 026662 012737 027026 000024 $PWRDN: MOV #SILLUP,@#PWRVEC ;;SET FOR FAST UP
(1) 026670 012737 000340 000026 MOV #340,@#PWRVEC+2 ;;PRIO:7
(3) 026676 010046 MOV R0,-(SP) ;;PUSH R0 ON STACK
(3) 026700 010146 MOV R1,-(SP) ;;PUSH R1 ON STACK
(3) 026702 010246 MOV R2,-(SP) ;;PUSH R2 ON STACK
(3) 026704 010346 MOV R3,-(SP) ;;PUSH R3 ON STACK
(3) 026706 010446 MOV R4,-(SP) ;;PUSH R4 ON STACK
(3) 026710 010546 MOV R5,-(SP) ;;PUSH R5 ON STACK
(3) 026712 017746 152222 MOV @SWR,-(SP) ;;PUSH @SWR ON STACK
(1) 026716 010637 027032 MOV SP,$SAVR6 ;;SAVE SP
(1) 026722 012737 026734 000024 MOV #SPWRUP,@#PWRVEC ;;SET UP VECTOR
(1) 026730 000000 HALT
(1) 026732 000776 BR .-2 ;;HANG UP
(1)
(2)
(1)
(1) 026734 012737 027026 000024 $PWRUP: MOV #SILLUP,@#PWRVEC ;;SET FOR FAST DOWN
(1) 026742 013706 027032 MOV $SAVR6,SP ;;GET SP
(1) 026746 005037 027032 CLR $SAVR6 ;;WAIT LOOP FOR THE TTY
(1) 026752 005237 027032 1$: INC $SAVR6 ;;WAIT FOR THE INC
(1) 026756 001375 BNE 1$ ;;OF WORD
(3) 026760 012677 152154 MOV (SP)+,@SWR ;;POP STACK INTO @SWR
(3) 026764 012605 MOV (SP)+,R5 ;;POP STACK INTO R5
(3) 026766 012604 MOV (SP)+,R4 ;;POP STACK INTO R4
(3) 026770 012603 MOV (SP)+,R3 ;;POP STACK INTO R3
(3) 026772 012602 MOV (SP)+,R2 ;;POP STACK INTO R2
(3) 026774 012601 MOV (SP)+,R1 ;;POP STACK INTO R1
(3) 026776 012600 MOV (SP)+,R0 ;;POP STACK INTO R0
(1) 027000 012737 026662 000024 MOV #SPWRDN,@#PWRVEC ;;SET UP THE POWER DOWN VECTOR
(1) 027006 012737 000340 000026 MOV #340,@#PWRVEC+2 ;;PRIO:7
(1) 027014 104401 TYPE ;;REPORT THE POWER FAILURE
(1) 027016 027034 $PWRMG: .WORD PWRMSG ;;POWER FAIL MESSAGE POINTER
(1) 027020 012716 MOV (PC)+,(SP) ;;RESTART AT START
(1) 027022 001726 $PWRAD: .WORD START ;;RESTART ADDRESS
(1) 027024 000002 RTI
(1) 027026 000000 $SILLUP: HALT ;;THE POWER UP SEQUENCE WAS STARTED
(1) 027030 000776 BR .-2 ;; BEFORE THE POWER DOWN WAS COMPLETE
(1) 027032 000000 $SAVR6: 0 ;;PUT THE SP HERE
3747 027034 015 012 PWRMSG: .BYTE 15,12
3748 027036 042522 052123 051101 .ASCII /RESTARTING AFTER A POWER FAILURE/
027044 044524 043516 040440
027052 052106 051105 040440
027060 050040 053517 051105
027066 043040 044501 052514
027074 042522
3749 027076 015 012 012 .BYTE 15,12,12,0
027101 000
3750 .EVEN
3751 .SBTTL TRAP DECODER
(1)
(2)
(1)
(1)

```

```

*****
*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS

```

```
(1)
(1)
(1)
(1) 027102 010046
(1) 027104 016600 000002
(1) 027110 005740
(1) 027112 111000
(1) 027114 006300
(1) 027116 016000 027136
(1) 027122 000200
(1)
(1)
(1)
(1)
(1) 027124 011646
(1) 027126 016666 000004 000002
(1) 027134 000002
(1)
(3)
(3)
(3)
(3)
(3)
(3)
(3)
(3)
(3) 027136 027124
(3) 027140 026132
(3) 027142 024100
(3) 027144 024054
(3) 027146 024114
(3) 027150 024636
(1)
(3) 027152 025426
(1)
(3) 027154 025356
(3) 027156 025640
(3) 027160 025760
(3) 027162 025254
3752 027164 023700
3753 027166 005015 046103 041517
      027174 040513 051440 020122
      027202 052506 041516 044524
      027210 047117 042440 051122
      027216 051117 000
3754 027221 015 041412 047514
      027226 045503 020101 051123
      027234 042040 052101 020101
      027242 051105 047522 000122
3755 027250 005015 046103 041517
      027256 040513 041040 020122
      027264 040504 040524 042440
      027272 051122 051117 000
3756 027277 015 041412 047514
      027304 045503 020101 051103
      027312 042040 052101 020101
      027320 051105 047522 000122
```

```
;*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL  
;*GO TO THAT ROUTINE.
```

```
$TRAP: MOV RO,-(SP) ;;SAVE R0
      MOV 2(SP),RO ;;GET TRAP ADDRESS
      TST -(RO) ;;BACKUP BY 2
      MOVB (RO),RO ;;GET RIGHT BYTE OF TRAP
      ASL RC ;;POSITION FOR INDEXING
      MOV $TRPAD(RO),RO ;;INDEX TO TABLE
      RTS RO ;;GO TO ROUTINE
```

```
;;THIS IS USE TO HANDLE THE 'GETPRI' MACRO
```

```
$TRAP2: MOV (SP),-(SP) ;;MOVE THE PC DOWN
        MOV 4(SP),2(SP) ;;MOVE THE PSW DOWN
        RTI ;;RESTORE THE PSW
```

```
.SBTTL TRAP TABLE
```

```
;*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED  
;*BY THE 'TRAP' INSTRUCTION.
```

```
: ROUTINE  
:-----
```

```
$TRPAD: .WORD $TRAP2
        $TYPE ;;CALL=TYPE TRAP+1(104401) TTY TYPEOUT ROUTINE
        $TYPOC ;;CALL=TYPOC TRAP+2(104402) TYPE OCTAL NUMBER (WITH LEADING ZEROS)
        $TYPOS ;;CALL=TYPOS TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)
        $TYPON ;;CALL=TYPON TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)
        $TYPDS ;;CALL=TYPDS TRAP+5(104405) TYPE DECIMAL NUMBER (WITH SIGN)
$GTSWR ;;CALL=GTSWR TRAP+6(104406) GET SOFT-SWR SETTING
$CKSWR ;;CALL=CKSWR TRAP+7(104407) TEST FOR CHANGE IN SOFT-SWR
$RDCHR ;;CALL=RDCHR TRAP+10(104410) TTY TYPEIN CHARACTER ROUTINE
$RDLIN ;;CALL=RDLIN TRAP+11(104411) TTY TYPEIN STRING ROUTINE
$RDOCT ;;CALL=RDOCT TRAP+12(104412) READ AN OCTAL NUMBER FROM TTY
IOTRD ;;CALL=IOTT TRAP+13(104413)
EM1: .ASCIIZ <15><12>/CLOCKA SR FUNCTION ERROR/
EM2: .ASCIIZ <15><12>/CLOCKA SR DATA ERROR/
EM3: .ASCIIZ <15><12>/CLOCKA BR DATA ERROR/
EM4: .ASCIIZ <15><12>/CLOCKA CR DATA ERROR/
```

3757	027326	005015	046103	041517	EM5:	.ASCIZ	<15><12>/CLOCKB SR DATA ERROR/
	027334	041113	051440	020122			
	027342	040504	040524	042440			
	027350	051122	051117	000			
3758	027355	015	041412	047514	EM6:	.ASCIZ	<15><12>/CLOCKB BR DATA ERROR/
	027362	045503	020102	051102			
	027370	042040	052101	020101			
	027376	051105	047522	000122			
3759	027404	005015	046103	041517	EM7:	.ASCIZ	<15><12>/CLOCKB CR DATA ERROR/
	027412	041113	041440	020122			
	027420	040504	040524	042440			
	027426	051122	051117	000			
3760	027433	015	042012	040525	EM10:	.ASCIZ	<15><12>/DUAL ADDRESS ERROR/
	027440	020114	042101	051104			
	027446	051505	020123	051105			
	027454	047522	000122				
3761	027460	005015	046103	041517	EM11:	.ASCIZ	<15><12>#CLOCK A COUNT ERROR #
	027466	020113	020101	047503			
	027474	047125	020124	051105			
	027502	047522	020122	000			
3762	027507	015	041412	047514	EM12:	.ASCIZ	<15><12>#CLOCK A COUNT FUNCTION ERROR #
	027514	045503	040440	041440			
	027522	052517	052116	043040			
	027530	047125	052103	047511			
	027536	020116	051105	047522			
	027544	020122	000				
3763	027547	015	041412	047514	EM14:	.ASCIZ	<15><12>#CLOCK B COUNT FUNCTION ERROR #
	027554	045503	041040	041440			
	027562	052517	052116	043040			
	027570	047125	052103	047511			
	027576	020116	051105	047522			
	027604	020122	000				
3764	027607	015	041412	047514	EM15:	.ASCIZ	<15><12>#CLOCK B COUNT ERROR #
	027614	045503	041040	041440			
	027622	052517	052116	042440			
	027630	051122	051117	000040			
3765	027636	005015	046103	041517	EM16:	.ASCIZ	<15><12>#CLOCK A INTERRUPT ERROR #
	027644	020113	020101	047111			
	027652	042524	051122	050125			
	027660	020124	051105	047522			
	027666	020122	000				
3766	027671	015	041412	047514	EM17:	.ASCIZ	<15><12>#CLOCK B INTERRUPT ERROR #
	027676	045503	041040	044440			
	027704	052116	051105	052522			
	027712	052120	042440	051122			
	027720	051117	000040				
3767	027724	005015	046103	041517	EM20:	.ASCIZ	<15><12>#CLOCK A REPEATABILITY ERROR #
	027732	020113	020101	042522			
	027740	042520	052101	041101			
	027746	046111	052111	020131			
	027754	051105	047522	020122			
	027762	000					
3768	027763	015	041412	047514	EM23:	.ASCIZ	<15><12>#CLOCK B REPEATABILITY ERROR #
	027770	045503	041040	051040			
	027776	050105	040505	040524			
	030004	044502	044514	054524			


```

(2) 031162 001376          BNE      2$
(2) 031164 012777 104000 150444 25$: MOV      #BIT15:BIT11,@KMADO ;SET RUN, AND ENABLE ARBITRATION.
(2) 031172 105201          INCB     R1
(2) 031174 001376          BNE      25$
(2)
(2) 031176 032777 000040 150432  BIT      #BITS,@KMADO ;SLAVE READY? (READING IPBM SR)
(2) 031204 001401          BEQ      3$
(2)
(2) 031206 104000          ERROR
(2)
(2) 031210 012777 000004 150424 3$: MOV      #4,@KMAD2 ;READ FAST PATH
(2) 031216          4$:
(3) 031216 004537 032474          JSR      R5, $TOUT ;-TOUT-CHECK FOR TIMEOUT
(3)
(3) 031222 104000          ERROR ;/TIME-OUT ERROR
(3) ;/WE FAILED TO COMPLETE
(3) ;/CURRENT OPERATION.
(3) ;/CONTINUES IN THIS LOOP
(3) ;/WOULD MAKE US 'HANG' HERE
(3)
(3) 031224 000774          BR              4$
(3)
(2) 031226 122777 000377 150406  CMPB     #377,@KMAD2 ;/RETURNS HERE-FROM-TIMED OUT.
(2) 031234 001370          BNE      4$ ;WAIT TILL KMC DONE COMMAND.
(2) 031236 122777 000377 150402  CMPB     #377,@KMAD4 ;IF FAST PATH=377 THEN ERROR.
(2) 031244 001001          BNE      35$
(2) 031246 104000          ERROR ;IPBM ERROR (SLAVE SIDE)
(2) ;YOU MUST RUN IPBM DIAGNOSTIC.
(2)
(2) 031250 117737 150372 031530 35$: MOVB     @KMAD4,11$ ;GET THE VERSION NUMBER FROM DMC-1'
(2) 031256 005227 177777          INC      #-1
(2) 031262 001045          BNE      5$
(2) 031264 005227 177777          INC      #-1
(2) 031270 001042          BNE      5$
(3) 031272 104401 031300          TYPE     ,67$ ;:TYPE ASCIZ STRING
(3) 031276 000426          BR       66$ ;:GET OVER THE ASCIZ
(3) ;:67$: .ASCIZ <200>'M8200-YC (DMC) MICROCODE VERSION NUMBER = ''
(3) 66$:
(2) 031354 013746 031530          MOV      11$,-(SP)
(2) 031360 104403          TYPOS
(2) 031362 002 000          .BYTE   2,0
(3) 031364 104401 031372          TYPE     ,69$ ;:TYPE ASCIZ STRING
(3) 031370 000402          BR       68$ ;:GET OVER THE ASCIZ
(3) ;:69$: .ASCIZ <200>' ''
(3) 68$:
(2) 031376 112737 177777 031530 5$: MOVB     #0-1,11$ ;DAC CODE FOR SLAVE.
(2) 031404 012501          MOV      (5)+,R1 ;GET NEXT DEVICE ADDR.
(2) 031406 021127 000000          CMP      (R1),#0 ;TERM REACHED?
(2) 031412 001444          BEQ      10$
(2) 031414 105237 031530          INCB     11$
(2) 031420 113777 031530 150220  MOVB     11$,@KMAD4 ;FIFO DATA
(2) 031426 004737 031532          JSR      PC,20$ ;ISSUE SEND
(2) 031432 112177 150210          MOVB     (R1)+,@KMAD4 ;SEND LOW BYTE OF DEVICE ADDR TO SLAVE.
(2) 031436 004737 031532          JSR      PC,20$ ;ISSUE SEND

```



```
(2) ;* ;RETURNS HERE
(2) ;* NOTE: MICRO CODE FILE MUST END IN -1 DATA.
(2) ;*
(2) $LOAD: MOV R4,-(SP) ;SAVE R4.
(2) 031564 010446 MOV R0,-(SP) ;SAVE R0.
(2) 031566 010046 1$: MOV (5)+,R0 ;GET PROG. ADDR.
(2) 031570 012500 CLR @KMAD0 ;CLEAR CSR
(2) 031572 005077 150040 CLR @KMAD4 ;CLEAR CRAM ADDR.
(2) 031576 005077 150044 2$: BIS #2000,@KMAD0 ;SELECT CRAM.
(2) 031602 052777 002000 150026 MOV (0)+,@KMAD6 ;WRITE DATA.
(2) 031610 012077 150036 BIS #20000,@KMAD0 ;SET CRAM WRITE
(2) 031614 052777 020000 150014 CLR @KMAD0 ;DISABLE CRAM.
(2) 031622 005077 150010 INC @KMAD4 ;UPDATE CRAM ADDR.
(2) 031626 005277 150014 CMP (0),#-1 ;ALL DONE?
(2) 031632 021027 177777 BNE 2$ ;NO LOOP.
(2) 031636 001361 CLR @KMAD4 ;CLEAR CRAM ADDR.
(2) 031640 005077 150002 MOV -2(5),R0 ;GET MICRO CODE ADDR.
(2) 031644 016500 177776
(2) 031650 052777 002000 147760 3$: BIS #2000,@KMAD0 ;SELECT CRAM
(2) 031656 022077 147770 CMP (R0)+,@KMAD6 ;DATA OK?
(2) 031662 001013 BNE 5$ ;NO - REPORT AN ERROR.
(2) 031664 021027 177777 CMP (0),#-1 ;ALL DONE?
(2) 031670 001405 BEQ 4$ ;YES - EXIT
(2) 031672 005077 147740 CLR @KMAD0 ;NO - DESELECT CRAM.
(2) 031676 005277 147744 INC @KMAD4 ;UPDATE CRAM ADDR.
(2) 031702 000762 BR 3$
(2) 4$: MOV (SP)+,R0 ;RESTORE R0
(2) 031704 012600 MOV (SP)+,R4 ;RESTORE R4
(2) 031706 012604 RTS R5 ;EXIT
(2) 031710 000205
(2) 5$: ;COME HERE ON LOAD ERROR
(2) 031712 TST -(5)
(2) 031712 005745 INCB R4 ;UPDATE ERROR COUNTER.
(2) 031714 105204 BPL 1$ ;IF NOT TOO MANY, TRY AGAIN.
(2) 031716 100324 HALT ;MICRO CODE LOAD ERROR.
(2) 031720 000000 ;KMC-11 FAULT. YOU COULD TRY
(2) 031722 000722 BR 1$ ;TO PRESS CONTINUE TO GIVE IT
;ANOTHER CHANCE, BUT I DOUBT
;THAT THAT WOULD WORK. SINCE I'VE
;ALREADY GIVEN IT 177 (OCTAL) CHANCES.
;TRY RUNNING THE KMC-11 DIAGNOSTIC.
(2)
(2) ;*THIS ROUTINE ISSUES A WRITE COMMAND TO THE LPA-11
(2) ;*
(2) CALL = JSR R5,$TLKW
(2) ;* .WORD 0 ;OFFSET OF DEVICE ADDR.
(2) ;* .WORD 0 ;DATA TO BE WRITTEN
(2)
(2) $TLKW: MOV R0,-(SP) ;SAVE R0
(2) 031724 010046 MOV (5)+,R0 ;GET DEVICE OFFSET
(2) 031726 012500 BIS #340,R0 ;ADD WRITE CODE.
(2) 031730 052700 000340 JSR PC,$LPW ;WAIT FOR FAST PATH READY
(2) 031734 004737 032206
```



```
(3) 032142 104000          ERROR          ;/TIME-OUT ERROR
(3)                          ;/WE FAILED TO COMPLETE
(3)                          ;/CURRENT OPERATION.
(3)                          ;/CONTINUES IN THIS LOOP
(3)                          ;/WOULD MAKE US 'HANG' HERE
(3) 032144 000774          BR              2$
(3)                          ;/RETURNS HERE-FROM-TIMED OUT.
(2) 032146 032777 000040 147462  BIT        #BIT5,@KMADO  ;FAST PATH READY?
(2) 032154 001370          BNE        2$
(2) 032156 112777 000004 147456  MOVB       #4,@KMAD2    ;ISSUE FAST PATH READ
(2) 032164 004737 032206          JSR        PC,$LPW
(2) 032170 117737 147452 032205  MOVB       @KMAD4,$DATR+1 ;SAVE HIGH BYTE
(2) 032176 012600          MOV        (SP)+,R0
(2) 032200 000205          RTS        R5
(2) 032202 000000          RD1:       0
(2) 032204 000000          $DATR:    .WORD    0
(2)                          ;
(2)                          ;THIS ROUTINE WAITS FOR KMC-CODE TO BECOME READY AS WELL
(2)                          ;AS FAST PATH TO BE READ.
(2)                          ;
(2)                          ;CALL = JSR    PC,$LPW
(2)                          ;
(2)                          ;IT WILL TIME OUT IF TOO MUCH TIME IS TAKEN BY
(2)                          ;THE MICRO-PROCESSORS AND REPORT AN ERROR, THEN HALT.
(2)                          ;
(2) 032206 010146          $LPW:     MOV        R1,-(SP)    ;SAVE R1
(2) 032210 005001          CLR        R1
(2) 032212 122777 000377 147422 1$:      CMPB       #377,@KMAD2  ;FINISHED INSTRUCTION?
(2) 032220 001403          BEQ        2$
(2) 032222 005201          INC        R1          ;TIME OUT?
(2) 032224 001372          BNE        1$
(2) 032226 000411          BR         10$
(2) 032230 032777 000020 147400 2$:      BIT        #BIT4,@KMADO  ;FAST PATH READ?
(2) 032236 001403          BEQ        3$
(2) 032240 005201          INC        R1          ;NO - TIME OUT?
(2) 032242 001372          BNE        2$
(2) 032244 000402          BR         10$          ;YES - REPORT AN ERROR
(2) 032246 012601          3$:      MOV        (SP)+,R1    ;RESTORE R1
(2) 032250 000207          RTS        PC          ;EXIT
(2) 032252
(3) 032252 104401 032260          10$:     TYPE        ,65$      ;;TYPE ASCIZ STRING
(3) 032256 000407          BR         64$          ;;GET OVER THE ASCIZ
(3)                          ;;65$:    .ASCIZ    <200>#LPA-11 FAULT#
(3) 032276          64$:
(2) 032276 000000          11$:     HALT
(2) 032300 000776          BR         11$          ;LPA-11 FAULT RUN LPA-11
(2)                          ;DIAGNOSTICS.
(2)
(2)
```

```

(2)
(2)
(2)
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(2)
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(2)
(2)
(2) 032302 010046
(2) 032304 010146
(2)
(2) 032306 012700 001664
(2) 032312 005001
(2) 032314 005710
(2) 032316 001421
(2) 032320 027520 000000
(2) 032324 001402
(2) 032326 005201
(2) 032330 000771
(2)
(2) 032332 010137 032350
(2) 032336 005725
(2) 032340 013537 032352
(2) 032344 004537 031724
(2) 032350 000000
(2) 032352 000000
(2) 032354 012601
(2) 032356 012600
(2) 032360 000205
(2) 032362 017520 000000
(2) 032366 005010
(2) 032370 004537 031074
(2) 032374 001664
(2) 032376 000755

```

```

; *
; * THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE TO
; * A DEVICE ADDRESS ON THE I/O BUSS FOR WRITE ONLY.
; *
; * FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN USED
; * BEFORE. IF NOT WE HAVE TO INITIALIZE THE LPA WITH
; * THAT ADDRESS.
; * WHEN THE ADDR. IS KNOWN BY THE LPA, DO THE OUTPUT BY
; * $TLKW
; *

```

```

$OUTLP: MOV R0,-(SP) ;SAVE R0
MOV R1,-(SP) ;SAVE R1
MOV #.DVLS,R0 ;PROGRAM DEFINED LIST.
CLR R1
1$: TST (0) ;TERMINATOR REACHED?
BEQ 10$ ;YES NEXT STEP.
CMP @ (5),(0)+ ;MATCH WITH ADDR IN LIST?
BEQ 2$
INC R1
BR 1$

2$: MOV R1,3$ ;SAVE OFFSET, DEVICE KNOWN.
TST (5)+
MOV @ (5)+,4$ ;GET DATA TO BE WRITTEN
JSR R5,$TLKW ;DO WRITE
3$: .WORD 0 ;DEVICE OFFSET
4$: .WORD 0 ;DATA TO BE WRITTEN.
MOV (SP)+,R1
MOV (SP)+,R0
RTS R5
10$: MOV @ (5),(0)+ ;SAVE ADDR.
CLR (0)
JSR R5,$LPAI
.WORD .DVLS
BR 2$

```

```

; *
; * THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE
; * TO A DEVICE ADDR. ON THE I/O BUSS FOR READ ONLY.
; *
; * FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN
; * USED BEFORE. IF NOT, WE HAVE TO INITIALIZE THE LPA
; * WITH THE NEW ADDR.
; * WHEN THE ADDR IS KNOWN WE CAN DO OUTPUT THROUGH
; * $TLKR
; *
; * CALL THROUGH MOVEI DATA,ADDR.
; * WHICH EQUALS:
; * JSR R5,$INLP
; * .WORD XX ADDR OF DEVICE
; * .WORD YY ADDR TO STORE READ DATA.
; *

```

```

(2) 032400 010046
(2) 032402 010146
(2)

```

```

$INLP: MOV R0,-(SP) ;SAVE R0
MOV R1,-(SP) ;SAVE R1

```



```

(2)
(2) 032534 000005          $RESET:  RESET          ;RESET THE WORLD.
(3)
(3)
(2) 032546 005737 031562  ;*   MOV    @2$,1$  ;/READ DEVICE REG 2$,PUT DATA IN 1$.
(2) 032552 001004          TST    $AERR      ;IF NO ERROR,LOOP
(2) 032554 062737 000002 032570 BNE    10$        ;THERE WAS AN ERROR.
(2)                                ADD    #2,2$      ;UPDATE DEVICE ADDR.
(2)                                ;YOU SEE ,WE HAVE TO PROTECT OUR SELF!
(2)                                ;IF 2$ CONTAINED A VALID ADDR,WE
(2)                                ;MUST KEEP TRYING UNTIL WE GENERATE
(2)                                ;AN INVALID ADDR.
(2) 032562 000764          BR     $RESET
(2) 032564 000207          10$:  RTS    PC
(2) 032566 000000          1$:   .WORD  0      ;JUNK LOC.
(2) 032570 160000          2$:   .WORD  160000 ;DUMB ADDR. FORCES INIT OF DMC/KMC.
(2)
(2)
(2)                                ;SDELAY- ROUTINE TO GIVE A MINOR DELAY.
(2)                                ;IS NOT TIME DEPENDENT CODE SENCE
(2)                                ;NOT USED TO GET SPECIFIC TIME BUT
(2)                                ;JUST A LITTLE DELAY.
(2)
(2)                                ;
(2)                                ; THAT IS UNLESS A REAL TIME CLOCK IS PRESENT!
(2)                                ; THEN WE'LL GENERATE A TIME BETWEEN 16MS TO 32 MS
(2)
(2)                                ;
(2)                                ; CALL= JSR PC, SDELAY
(2)
(2)                                ;
(2) 032572          SDELAY:  TST    RTCCSR      ;CLOCK PRESENT?
(2) 032572 005737 032654          BPL    10$
(2) 032576 100016          MOV    #2,TIME
(2) 032600 012737 000002 032644  BIS    #115,@RTCCSR ;START CLOCK
(2) 032606 052777 000115 000040  CLR    PS
(2) 032614 005037 177776          1$:   TST    TIME
(2) 032620 005737 032644          BNE    1$
(2) 032624 001375          CLR    @RTCCSR      ;STOP CLOCK
(2) 032626 005077 000022
(2)
(2) 032632 000207          RTS   PC
(2) 032634 105237 032644          10$:  INCB   TIME
(2) 032640 001375          BNE   10$
(2) 032642 000207          RTS   PC
(2)
(2) 032644 000000          TIME: .WORD  0
(2)
(2) 032646 005337 032644          CLKINT: DEC    TIME
(2) 032652 000002          RTI
(2) 032654 000000          RTCCSR: .WORD  0      ;CLOCK CSR IF USED.
(2)
(2)
(2)                                ;*
(2)                                ;*THIS MACRO ALLOWS THE OPERATOR TO TALK TO
(2)                                ;*ANY DEVICE ON THE I/O BUS
(2)                                ;*USER MUST START AT THIS ADDR.
(2)                                ;*HE MUST SAY EITHER 'E' FOR EXAMINE, OR 'D' FOR DEPOSIT.
(2)

```

```

(2)                                     ;*'E' IS DEFAULT.
(2)                                     ;*NEXT, HE MUST SUPPLY AN ADDR.
(2)                                     ;*NOTE IF ADDR. IS NOT FOUND ON I/O BUS, A HALT
(2)                                     ;*WILL OCCUR.
(2)
(2) 032656                               $UTK:
(2) 032656 005037 001664                CLR      .DVLS
(2) 032662                               21$:
(3) 032662 104401 032670                TYPE    ,65$           ;;TYPE ASCIZ STRING
(3) 032666 000405                       BR      64$           ;;GET OVER THE ASCIZ
(3)                                     ;;65$: .ASCIZ <200>#E OR D?#
(3) 032702                               64$:
(2) 032702 105777 146236                1$:  TSTB    @STKS
(2) 032706 100375                       BPL     1$
(2) 032710 117737 146232 033032         MOVB    @STKB,20$     ;GET INPUT
(2) 032716 104401 033032                 TYPE    ,20$         ;ECHO, NEXT MESSAGE.
(2) 032722 142737 000240 033032         BICB    #240,20$     ;STRIP PARITY, LC
(2) 032730 104412                       RDOCT
(2) 032732 012637 033030                 MOV     (SP)+,14$    ;GET ADDR.
(2) 032736 123727 033032 000104         CMPB    20$,#D      ;DEPOSIT?
(2) 032744 001411                       BEQ     10$
(2)
(2) 032746 004537 032400                JSR     R5,$INLP     ;GET DATA
(2) 032752 033030                               2$:  .WORD   14$
(2) 032754 032766                       .WORD   5$
(2)
(3) 032756 013746 032766                MOV     5$,-(SP)    ;;SAVE 5$ FOR TYPEOUT
(3) 032762 104402                       TYPOC
(2) 032764 000736                       BR      21$         ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
(2) 032766 000000                               5$:  .WORD   0        ;LOOP.
(2)
(2) 032770                               10$:
(2) 032770 104401 032776                TYPE    ,67$           ;;TYPE ASCIZ STRING
(3) 032774 000404                       BR      66$           ;;GET OVER THE ASCIZ
(3)                                     ;;67$: .ASCIZ <200>#DATA= #
(3) 033006                               66$:
(2) 033006 104412                       RDOCT
(2) 033010 012637 033026                 MOV     (SP)+,13$
(2)
(2) 033014 004537 032302                11$: JSR     R5,$OUTLP   ;OUTPUT ROUTINE.
(2) 033020 033030                               12$: .WORD   14$     ;DEVICE ADDR.
(2) 033022 033026                       .WORD   13$     ;DATA
(2) 033024 000716                       BR      21$
(2)
(2) 033026 000000                               13$: .WORD   0
(2) 033030 000000                               14$: .WORD   0
(2) 033032 100001 042504 044526         20$: .ASCIZ  <1><200>#DEVICE ADDR= #
(2) 033040 042503 040440 042104
(2) 033046 036522 000040
(2)
(2)                                     .EVEN
(1)
(1)
(2)
(2)                                     ;
(2)                                     ;THIS ROUTINE LOOKS THROUGH CURENT .DVLS FOR A/D ADDR.
(2)                                     ;IF UNFOUND,GENERATES IT. THIS ROUTINE'S WHOLE PURPOSE IS

```

```

(2) ;TO SET UP THE USER PROGRAM TO LINK TO FILE 'DRLPX2' FOR
(2) ;SAMPLE TAKEING PURPOSES.
(2) TO TAKE SAMPLES, THE USER PROGRAM MUST SET UP
(2) A/D CSR IN BSEL 4, AND 5.
(2) (2) HE MUST CALL THIS ROUTINE:
(2) JSR R5,$PUTS ;CALL SET UP ROUTINE.
(2) .WORD ADCSR ;ADDR. OF A/D CSR.
(2) ;RETURNS HERE ;KMC BSEL 3,6,7 PERMINENTLY SET UP
(2) ;(UNTILL ONE DOES A RESET)
(2)
(2) (3)THE USER MUST PUT CODE 006 INTO KMC REG 2 TO
(2) START CONVERSION CAUTION*DO WITH MOVB INSTR.!
(2) (4)MONITOR KMC REG 2 FOR CODE 377 (DRLPX2 IS DONE)
(2) (5)READ KMC REG 4,5 FOR A/D RESULT.
(2) (6) TO TAKE MORE SAMPLES, SIMPLY PUT A/D CSR INTO
(2) BSEL 4,5 AND CODE 6 INTO BSEL 2.
(2)
(2) $PUTS: MOV (5)+,1$ ;GET ADDR OF ADDR. OF A/D
(2) JSR R5,$INLP
(2) 1$: .WORD 0
(2) .WORD 10$
(2) MOVB $OFS,@KMA6
(2) MOVB $OFS,@KMA7
(2) MOV 1$,2$
(2) ADD #2,2$
(2) JSR R5,$INLP
(2) 2$: .WORD 0
(2) .WORD 10$
(2) MOVB $OFS,@KMA3
(2) BISB #340,@KMA6
(2) BISB #300,@KMA7
(2) BISB #300,@KMA5
(2) RTS R5
(2) 10$: .WORD 0
(2)
3806
3807 042000 .=42000
3808 ;HERE RESIDES THE MICRO-CODE USED BY THE PROGRAM
3809 043000 .=43000
3810 ;FREE LOCATION AFTER THE MICRO-CODE
3811
3812 000001 .END
  
```

ABASE = 170404	1221#	1279												
ABR 001326	1279#	1462*	1518	1548	1549	1576	1577	1778	1797	1825	1853	2040	2092	
	2150	2202	2281	2282	2283	2284	2285	2286	2304	2350	2356	2391	2431	
	2548	2549	2593	2594	2618	2672	2685	2735	3084	3148	3258	3259	3260	
	3261	3520	3615	3788										
ACDW1 = 000000	1279													
ACDW2 = 000000	1279													
ACPUOP= 000000	1279													
ACR 001330	1279#	1464*	1518	1801	1826	1854	2052	2109	2219	2281	2282	2283	2284	
	2285	2286	2312	2360	2437	2593	2594	2622	2699	2742	2987	3096	3155	
	3258	3259	3260	3261	3527	3789	3796	3797						
ADDW0 = 000000	1279													
ADDW1 = 000000	1279													
ADDW10= 000000	1279													
ADDW11= 000000	1279													
ADDW12= 000000	1279													
ADDW13= 000000	1279													
ADDW14= 000000	1279													
ADDW15= 000000	1279													
ADDW2 = 000000	1279													
ADDW3 = 000000	1279													
ADDW4 = 000000	1279													
ADDW5 = 000000	1279													
ADDW6 = 000000	1279													
ADDW7 = 000000	1279													
ADDW8 = 000000	1279													
ADDW9 = 000000	1279													
ADEVCT= 000000	1279													
ADEVN = 000000	1279													
AENV = 000000	1279													
AENVN = 000000	1279													
AFATAL= 000000	1279													
AMADH1= 000000	1279													
AMADR2= 000000	1279													
AMADR3= 000000	1279													
AMADR4= 000000	1279													
AMAMS1= 000000	1279													
AMAMS2= 000000	1279													
AMAMS3= 000000	1279													
AMAMS4= 000000	1279													
AMSGAD= 000000	1279													
AMSGLG= 000000	1279													
AMSGTY= 000000	1279													
AMTYP1= 000000	1279													
AMTYP2= 000000	1279													
AMTYP3= 000000	1279													
AMTYP4= 000000	1279													
APASS = 000000	1279													
APRIOR= 000006	1223#	1279												
APRITY 001350	1279#	1480												
APTC SU= 000040	3744	3745#												
APTENV= 000001	3738	3744	3745#											
APTSIZ= 000200	1444	3745#												
APTSPO= 000100	3744	3745#												
ASR 001324	1279#	1450*	1460	1518	1609	1610	1620	1778	1796	1820	1844	1971	1972	
	1976	1979	2004	2005	2007	2008	2020	2039	2046	2047	2049	2091	2099	

TST12	003354	1778#
TST120	014600	2651#
TST121	015016	2724#
TST122	015164	2776#
TST123	015314	2827#
TST124	015522	2893#
TST125	015712	2943#
TST126	016006	2968#
TST127	016106	3048#
TST13	003454	1778#
TST130	016226	3049#
TST131	016346	3050#
TST132	016466	3051#
TST133	016606	3052#
TST134	016726	3053#
TST135	017046	3064#
TST136	017240	3136#
TST137	017352	3258#
TST14	003554	1778#
TST140	017642	3259#
TST141	020132	3260#
TST142	020422	3261#
TST143	020712	3362#
TST144	021216	3363#
TST145	021522	3364#
TST146	022026	3365#
TST15	003654	1778#
TST16	003754	1778#
TST17	004054	1778#
TST2	002602	1542#
TST20	004154	1778#
TST21	004254	1778#
TST22	004354	1778#
TST23	004454	1778#
TST24	004554	1778#
TST25	004654	1778#
TST26	004754	1778#
TST27	005054	1778#
TST3	002642	1571#
TST30	005154	1778#
TST31	005254	1778#
TST32	005354	1778#
TST33	005454	1778#
TST34	005554	1778#
TST35	005654	1778#
TST36	005754	1778#
TST37	006054	1778#
TST4	002700	1604#
TST40	006154	1778#
TST41	006254	1778#
TST42	006354	1778#
TST43	006454	1778#
TST44	006554	1778#
TST45	006654	1778#
TST46	006754	1778#
TST47	007054	1778#

ADTST	1493#	1518													
AREPT	3263#														
BREPT	3367#														
BRTM	2997#	3048	3049	3050	3051	3052	3053								
CADT	3169#	3258	3259	3260	3261										
CADTB	3288#	3362	3363	3364	3365										
CBC	1778#														
CBTC	2558#	2593	2594												
CBT25	2494#	2548	2549												
COMMEN	1220#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809	1832
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056	2063
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284	2285
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593	2594
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922	2929
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159	3165
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586	3635
	3639	3690	3694	3724	3730										
CSRDTA	1680#	1778													
DFC	1280#	1790	1297	1304	1311	1318	1325	1332	1340	1347	1354	1368	1375	1382	1396
	1403	1410	1417	1424	1431	1438									
ECALL	1717#	1778													
ECB	1254#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809	1832
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056	2063
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284	2285
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593	2594
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922	2929
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159	3165
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586	3635
	3639	3690	3694	3724	3730										
ENDCOM	1220#	1554	1557	1581	1584	1613	1617	1640	1644	1665	1669	1778	1805	1809	1832
	1837	1860	1865	1890	1894	1918	1923	1946	1951	1983	1987	2012	2017	2056	2063
	2114	2118	2163	2166	2174	2179	2213	2216	2223	2231	2281	2282	2283	2284	2285
	2286	2321	2326	2363	2367	2400	2403	2440	2452	2489	2491	2548	2549	2593	2594
	2625	2628	2688	2695	2704	2710	2748	2751	2797	2810	2865	2869	2919	2922	2929
	2932	2962	2965	2990	2994	3048	3049	3050	3051	3052	3053	3100	3111	3159	3165
	3258	3259	3260	3261	3362	3363	3364	3365	3476	3480	3531	3534	3583	3586	3635
	3639	3690	3694	3701	3724	3730									
ERROR	1220#	1555	1582	1614	1641	1666	1778	1806	1833	1861	1891	1919	1947	1984	2013
	2057	2115	2164	2175	2214	2224	2281	2282	2283	2284	2285	2286	2322	2364	2401
	2441	2490	2548	2549	2593	2594	2626	2689	2705	2749	2798	2866	2920	2930	2963
	2991	3048	3049	3050	3051	3052	3053	3101	3161	3258	3259	3260	3261	3362	3363
	3364	3365	3478	3532	3584	3636	3691	3805							
ESCAPE	1220#														
GETPRI	1220#														
GETSWR	1220#														
MOVEI	170#	1518	1549	1577	1610	1636	1661	1778	1801	1826	1854	1886	1912	1940	1972
	1979	2005	2008	2047	2052	2102	2109	2155	2160	2170	2205	2210	2219	2281	2282
	2283	2284	2285	2286	2312	2316	2346	2360	2394	2397	2434	2437	2470	2482	2486
	2548	2549	2593	2594	2619	2622	2677	2685	2699	2742	2745	2788	2791	2794	2855
	2861	2913	2916	2925	2958	2987	3048	3049	3050	3051	3052	3053	3093	3096	3149
	3155	3258	3259	3260	3261	3362	3363	3364	3365	3472	3523	3527	3567	3580	3622
	3632	3677	3687	3805											
MOVEM	157#	1548	1576	1609	1620	1635	1660	1778	1796	1797	1820	1825	1844	1853	1881
	1882	1902	1909	1930	1937	1971	1976	2004	2007	2020	2039	2040	2046	2049	2091
	2092	2099	2104	2148	2150	2154	2157	2194	2202	2204	2207	2281	2282	2283	2284
	2285	2286	2303	2304	2306	2349	2350	2352	2356	2389	2391	2393	2396	2429	2431

.TRMTR	1156#		
.UTK	699#	3805	
.\$ACT1	1159#	1275	
.\$APT8	1159#	1279#	
.\$APTH	1159#	1277	
.\$APTY	1159#	3745	
.\$CATC	1157#	1209	
.\$CMTA	1157#	1279	
.\$EOP	1158#	3395	
.\$ERRO	1158#	3738	
.\$ERRT	1158#	3739	
.\$INLP	652#	3805	
.\$MMAC	141#		
.\$OUTL	610#	3805	
.\$POWE	1157#	3746	
.\$RDOC	1156#	1159#	3742
.\$READ	1158#	3743	
.\$SCOP	1158#	3741	
.\$TLKW	511#	3805	
.\$TOUT	1439#	3805	
.\$TRAP	1156#	3751	
.\$TYPD	1156#	1158#	3740
.\$TYPE	1158#	3744	
.\$TYPO	1157#	3737	

. ABS.	043000	000	CON	RW	ABS	LCL	I
	000000	001	CON	RW	REL	LCL	I

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

CRLPGC,CRLPGC/CRF=CRLPAB.MAC,CRLPGC.P11
RUN-TIME: 42 36 1 SECONDS
RUN-TIME RATIO: 390/80=4.8
CORE USED: 42K (83 PAGES)

DRLPX2(IMAGE) MICRO CODE
CRLPX2.P11 02-NOV-79 11:22

:DEFAULT TITLE MACY11 30G(1063) 24-OCT-80 09:45 PAGE 1

SEQ 0202

:THIS FILE IS THE SAME AS 'CRLPX0.P11' EXCEPT IT IS LOADED INTO 65000
:IT IS ALSO THE SAME AS 'DRLPX2.P11' EXCEPT NAME CHANGE 'CRLPX2.P11'

1
2
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12
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452
453
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455
456
457
458

177777

000000'
000000

.LIST MC,BIN,BEX,MEB
.NLIST MD,CND,ME

ADDRESS=-1
MACRO DEFFINITIONS FOR M8200 AND M8204 MICRO-PROCESSOR
INSTRUCTION SET.
TO BE USED WITH RSX MACRO-11 ASSEMBLER

26-MAY-1976
\$BEGIN
\$LOC 42000
.GLOBL DRLPX2
.ENABL GBL

*
:*MICRO CODE FOR KMC-11

460
 461
 462
 463
 464
 465
 466 042000
 467 042000
 (2) 042000 100407
 468 042002
 (2) 042002 100420
 469 042004
 (2) 042004 100430
 470 042006
 (2) 042006 100432
 471 042010
 (2) 042010 100434
 472 042012
 (2) 042012 100436
 473 042014
 (2) 042014 100440
 474
 475
 476
 477
 478 042016
 479 042016
 (3) 042016 000400
 480 042020
 (3) 042020 061220
 481 042022
 (3) 042022 061222
 482 042024
 (3) 042024 061223
 483 042026
 (3) 042026 061224
 484 042030
 (3) 042030 061225
 485 042032
 (3) 042032 061226
 486 042034
 (3) 042034 061227
 487 042036
 (3) 042036 063226
 488
 489 042040
 (3) 042040 021240
 490 042042
 (3) 042042 000777
 491 042044
 (3) 042044 061222
 492
 493 042046
 (3) 042046 021240
 494
 495 042050

:*THIS CODE WILL BE DOWN LOADED INTO BOTH
 :*KMC-11'S. THE CODE RUNS ASYNCHRONOUS TO THE PDP-11 CODE
 :*WE SYNC THROUGH COMMANDS PASSED VIA THE OUT*/IBUS* REGS.
 :*

DRLPX2: ;JUMP TABLE USED FOR COMMANDS
 BR STARTU ;GOTO START
 .WORD .\$\$\$.
 BR CMNOP ;NOP=1
 .WORD .\$\$\$.
 BR RDSILO ;=2 READ SILO PUT IN BSEL4
 .WORD .\$\$\$.
 BR WRSILO ;=3 READ BSEL4 PUT IN SILO.
 .WORD .\$\$\$.
 BR RDCMND ;=4 READ FAST PATH PUT IN BSEL4
 .WORD .\$\$\$.
 BR WRCMND ;=5 READ BSEL4, PUT IN FAST PATH.
 .WORD .\$\$\$.
 BR SAMP ;=6 TAKE AN A/D SAMPLE
 .WORD .\$\$\$.
 ;START OF U CODED

STARTU: MOVE # 0,BREG
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <0> ;CLEAR UNIBUS CSRS
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <2>
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <3>
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <4>
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <5>
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <6>
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <7>
 .WORD .\$\$\$.
 MOVE BREG,SPAD <6>
 .WORD .\$\$\$.
 CMNOP: MOVE INP0 <12>,OUT1 <0> ;READ STATUS
 .WORD .\$\$\$.
 MOVE # 377,BREG
 .WORD .\$\$\$.
 MOVE BREG,OUT1 <2> ;INDICATE READY FOR COMMAND.
 .WORD .\$\$\$.
 LOOP: MOVE INP0 <12>,OUT1 <0> ;READ STATUS
 .WORD .\$\$\$.
 MOVE INP1 <2>,SPAD <0> ;READ COMMAND REG.

```
(3) 042050 123040 .WORD .$$$.  
496 042052 BZ LOOP ;NO COMMAND THEN LOOP  
(2) 042052 101423 .WORD .$$$.  
497  
498 042054 MOVE INP1 <2>,SPAD <0> ;RE-READ COMMAND.  
(3) 042054 123040 .WORD .$$$.  
499  
500 042056 BR SPAD <0> ;BR BASED ON CMND.  
(2) 042056 160600 .WORD .$$$.  
501 ;NO-USER PROTECTION OFFERED.  
502 ;IF YOU ENTER WRONG CODE -  
503 ;YOU LOSE.  
504  
505  
506 ;ROUTINE TO READ THE SILO, PUT IN  
507 ;*BUS REG 4  
508 ;CMD=2  
509  
510 RDSILO: MOVE INP0 <10>,OUT1 <4> ;READ SILO.  
(3) 042060 021204 .WORD .$$$.  
511 ;WRITE *BUS  
512 042062 BR CMNOP ;RETURN.  
(2) 042062 100420 .WORD .$$$.  
513  
514 ;ROUTINE TO WRITE SILO, READ DATA FROM  
515 ;*BUS REG 4  
516 ;CMD=3  
517  
518  
519  
520 WRSILO: MOVE INP1 <4>,OUT0 <10> ;READ DATA IN *BUS  
(3) 042064 122110 .WORD .$$$.  
521 ;WRITE SILO.  
522 042066 BR CMNOP  
(2) 042066 100420 .WORD .$$$.  
523  
524 ;ROUTINE TO READ FAST PATH (CMND) REG.  
525 ;PUT IN *BUS REG 4  
526 ;CMD=4  
527  
528  
529  
530 RDCMND: MOVE INP0 <11>,OUT1 <4> ;READ FAST PATH  
(3) 042070 021224 .WORD .$$$.  
531 ;WRITE *BUS.  
532 042072 BR CMNOP ;RETURN  
(2) 042072 100420 .WORD .$$$.  
533  
534 ;ROUTINE TO WRITE FAST PATH (CMND) REG.  
535 ;TAKE DATA FROM *BUS REG 4.  
536 ;CMD=5  
537  
538  
539  
540 WRCMND: MOVE INP1 <4>,OUT0 <11> ;READ DATA IN *BUS  
(3) 042074 122111 .WORD .$$$.
```

```

541                                     ;WRITE INTO FAST PATH.
542 042076 BR CMNOP ;RETURN.
(2) 042076 100420 .WORD .$$$.
```

543
544
545
546 ; THIS ROUTINE TAKES AN A/D SAMPLE.
547 ; CALL= CMND 6 IN BSEL2
548 ; THESE REGS. MUST BE SET UP IN ADVANCE.
549 ; BSEL 3 MUST CONTAIN READ CODE FOR A/D BUFFER.
550 ; BSEL 4,5 MUST CONTAIN A/D CSR SETTING.
551 ; BSEL 6 MUST CONTAIN WRITE CODE FOR A/D CSR
552 ; BSEL 7 MUST CONTAIN READ CODE FOR A/D CSR
553 ; BSEL 3,6,7 WILL REMAIN UNEFFECTED.
554 ; BSEL 4,5 WILL CONTAIN A/D SAMPLE.
555 ; BSEL2 WILL CONTAIN CODE 377 WHEN DONE.
556

```

567 042100 WTMC SAMP
(4) 042100 020640 .WORD .$$$.
```

```

(3) 042102 103040 .WORD .$$$.
```

```

568 042104 MOVE INP1 <6>,OUT0 <11> ;SEND A/D WRITE CODE.
(3) 042104 122151 .WORD .$$$.
```

```

569 042106 WTMC SAMP1
(4) 042106 020640 .WORD .$$$.
```

```

(3) 042110 103043 .WORD .$$$.
```

```

570 042112 MOVE INP1 <4>,OUT0 <11> ;SEND LOW BYTE CSR INFO.
(3) 042112 122111 .WORD .$$$.
```

```

571 042114 WTMC SAMP2
(4) 042114 020640 .WORD .$$$.
```

```

(3) 042116 103046 .WORD .$$$.
```

```

572 042120 MOVE INP1 <5>,OUT0 <11> ;SEND HIGH BYTE CSR INFO.
(3) 042120 122131 .WORD .$$$.
```

```

573 042122 WTMC SLOOP
(4) 042122 020640 .WORD .$$$.
```

```

(3) 042124 103051 .WORD .$$$.
```

```

574 042126 MOVE INP1 <7>,OUT0 <11> ;SEND READ CODE TO GET A/D CSR.
(3) 042126 122171 .WORD .$$$.
```

```

575 042130 WTMC SAMP3
(4) 042130 020640 .WORD .$$$.
```

```

(3) 042132 103054 .WORD .$$$.
```

```

576 042134 WTMM SLOOP1
(4) 042134 020640 .WORD .$$$.
```

```

(4) 042136 061620 .WORD .$$$.
```

```

(3) 042140 103056 .WORD .$$$.
```

```

577 042142 MOVE INP0 <11>,.BREG
(3) 042142 020620 .WORD .$$$.
```

```

578 042144 MOVE BREG,SPAD <0>
(3) 042144 063220 .WORD .$$$.
```

```

579 042146 WTMM SLOOP2
(4) 042146 020640 .WORD .$$$.
```

```

(4) 042150 061620 .WORD .$$$.
```

```

(3) 042152 103063 .WORD .$$$.
```

```

580 042154 MOVE INP0 <11>,.BREG
(3) 042154 020620 .WORD .$$$.
```

```

581 042156 BB7 CMNOP ;ABORT IF A/D BIT 15=1
```


(2)	042156	103420	.WORD	.\$\$\$.	
582	042160		MOVE	SPAD <0>,BREG	
(3)	042160	060600	.WORD	.\$\$\$.	
583	042162		BB7	LOPE	
(2)	042162	103473	.WORD	.\$\$\$.	
584	042164		BR	SLOOP	:IF A/D NOT DONE,EXIT.
(2)	042164	100451	.WORD	.\$\$\$.	
585	042166		LOPE: MOVE	INP1 <3>,OUT0 <11>	:ISSUE READ A/B BUFFER.
(3)	042166	122071	.WORD	.\$\$\$.	
586	042170		WTMM	SLOOP3	
(4)	042170	020640	.WORD	.\$\$\$.	
(4)	042172	061620	.WORD	.\$\$\$.	
(3)	042174	103074	.WORD	.\$\$\$.	
587	042176		MOVE	INP0 <11>,OUT1 <4>	
(3)	042176	021224	.WORD	.\$\$\$.	
588	042200		WTMM	SLOOP4	
(4)	042200	020640	.WORD	.\$\$\$.	
(4)	042202	061620	.WORD	.\$\$\$.	
(3)	042204	103100	.WORD	.\$\$\$.	
589	042206		MOVE	INP0 <11>,OUT1 <5>	
(3)	042206	021225	.WORD	.\$\$\$.	
590	042210		BR	CMNOP	
(2)	042210	100420	.WORD	.\$\$\$.	
591	042212	177777	.WORD	-1	
592		000001	.END		

ADDRES= 177777	SAMP 042100	.ADDWC= 000020	.DMEM = 002400	.SELB = 000220
CLK = 000020	SAMP1 042106	.AND = 000260	.DNOP = 000000	.SIMP = 000000
CMNOP 042040	SAMP2 042114	.BB0 = 002000	.DOUT0= 002000	.SINO = 020000
DRLPX2 042000 G	SAMP3 042130	.BB1 = 002400	.DOUT1= 001000	.SIN1 = 120000
LOOP 042046	SLOOP 042122	.BB4 = 003000	.DSPAD= 003000	.SMEM = 040000
LOPE 042166	SLOOP1 042134	.BB7 = 003400	.DSPBR= 003400	.SUB = 000340
MARHLD= 000000	SLOOP2 042146	.BC = 001000	.DO = 000400	.SUBWC= 000040
MARINC= 014000	SLOOP3 042170	.BR = 000400	.FO = 000020	.SUB2C= 000360
MARLD = 010000	SLOOP4 042200	.BSBRG= 160000	.INC = 000060	.SO = 020000
MARLDX= 004000	STARTU 042016	.BSIMM= 100000	.LORN = 000240	.XOR = 000320
PAGE0 = 000000	WRCMND 042074	.BSMEM= 140000	.MINUS= 000360	.\$\$\$ = 100420
PAGE1 = 001000	WRSILO 042064	.BZ = 001400	.MO = 004000	..LOC = 042040
PAGE2 = 002000	\$\$\$\$SER= 000001	.CO = 000400	.OR = 000300	.2A = 000120
PAGE3 = 003000	. = 042214	.DBR = 000400	.PLUS = 000000	.2AUC = 000140
RDCMND 042070	.ADC = 000100	.DBRSH= 001400	.SBREG= 060000	
RDSILO 042060	.ADD = 000000	.DEC = 000160	.SELA = 000200	

. ABS.	042214	000	OVR	RW	ABS	LCL	D
	000000	001	CON	RW	ABS	LCL	I
ABCODE	004000	002	CON	RW	REL	LCL	I

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

CRLPX2,CRLPX2=CRLPX2
 RUN-TIME: 3 3 0 SECONDS
 RUN-TIME RATIO: 49/7=6.5
 CORE USED: 42K (83 PAGES)